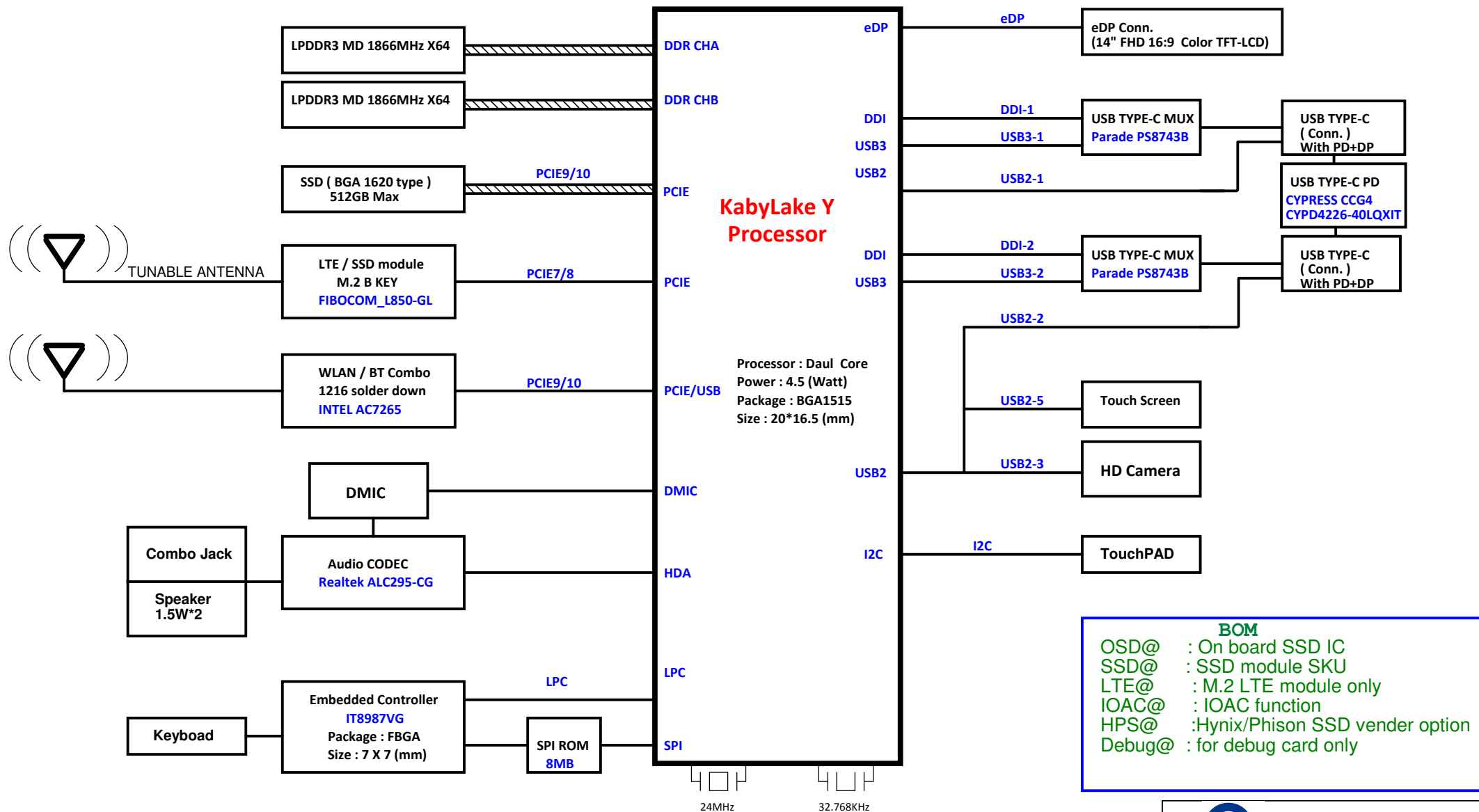
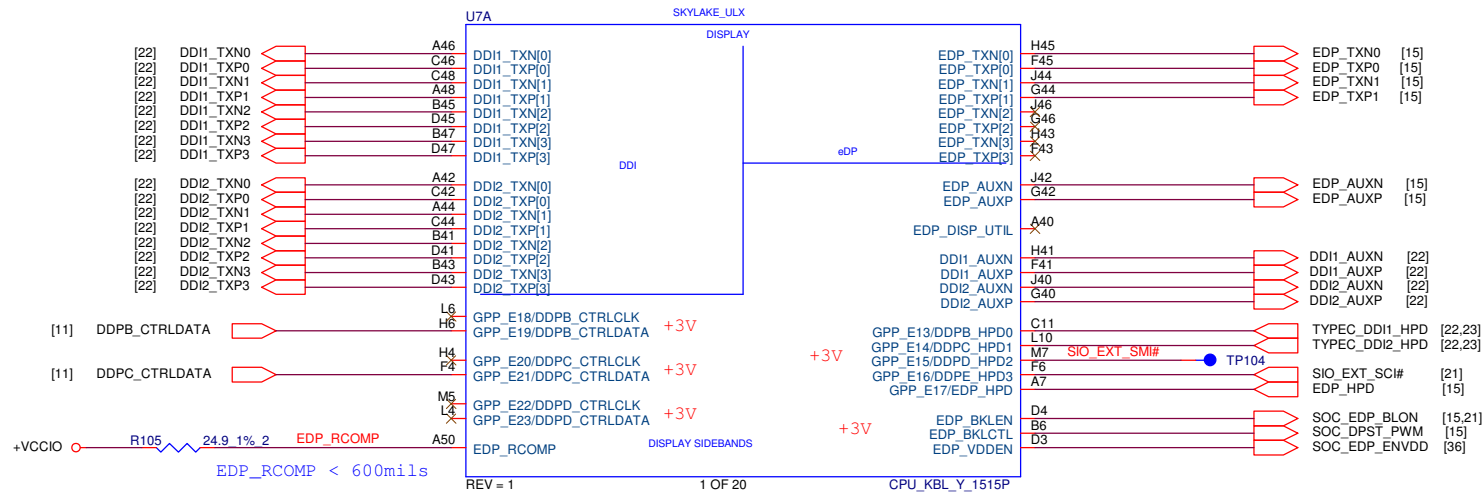


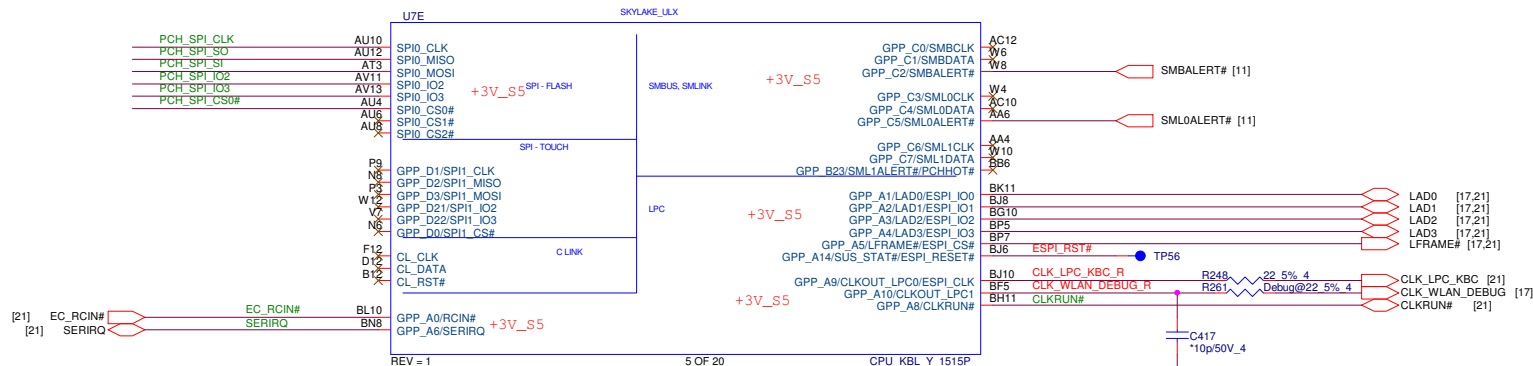
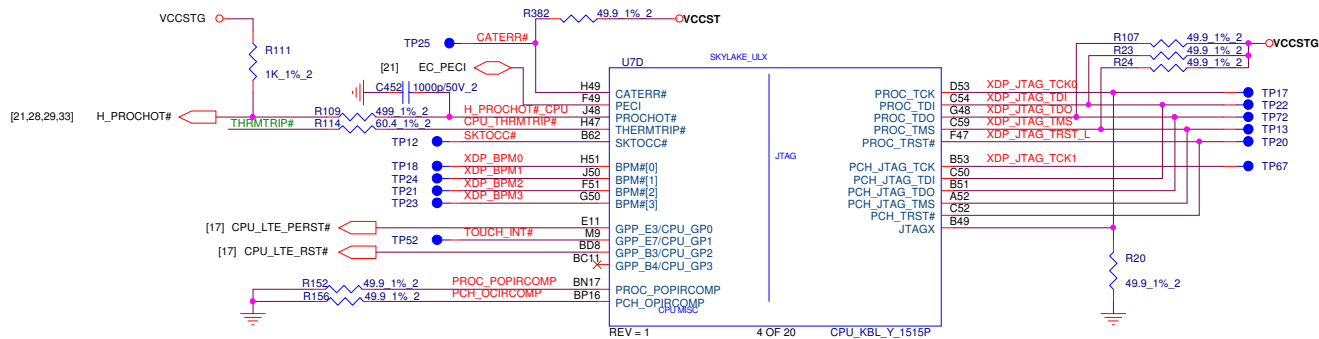
ZDJ System Block Diagram



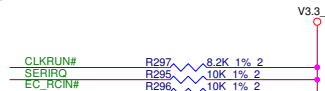


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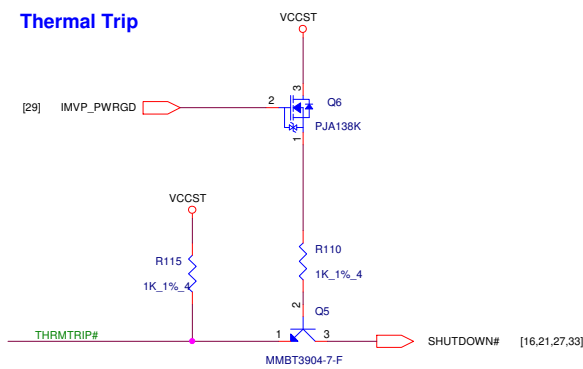
Size	Document Number	Rev
	KBL-Y CPU (DDI/EDP)	2A
Date:	Monday, January 22, 2018	Sheet 2 of 39



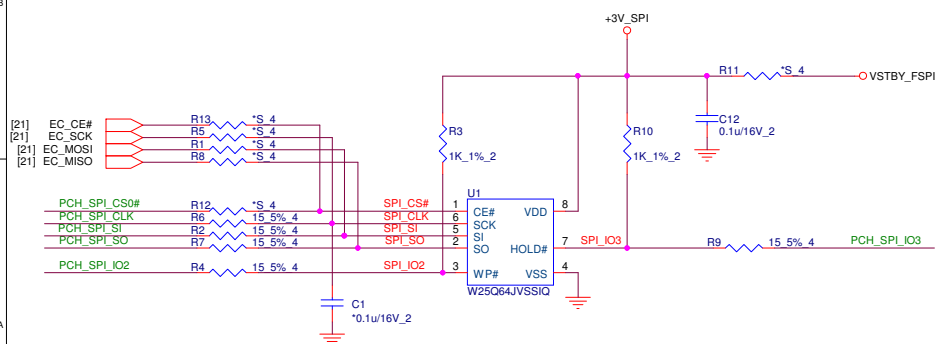
PU/PD



Thermal Trip



SPI ROM for EC & BIOS



socket P/N: DG008000011 only for A-TEST
Normal PN : AKE3EZ-0N01




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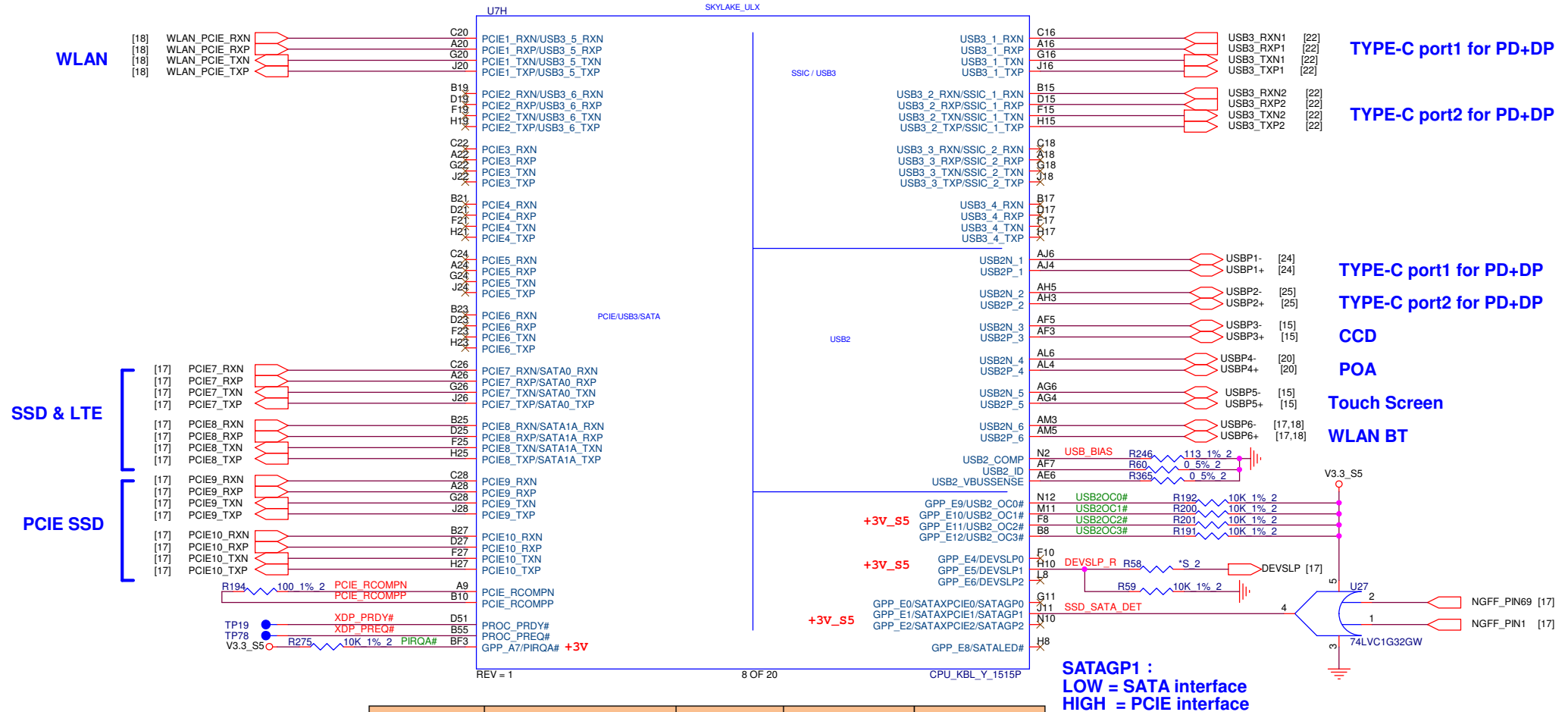
PROJECT : ZDJ

Size	Document Number	Rev
	KBL-Y CPU (MISC/SPI/SMB))	2A

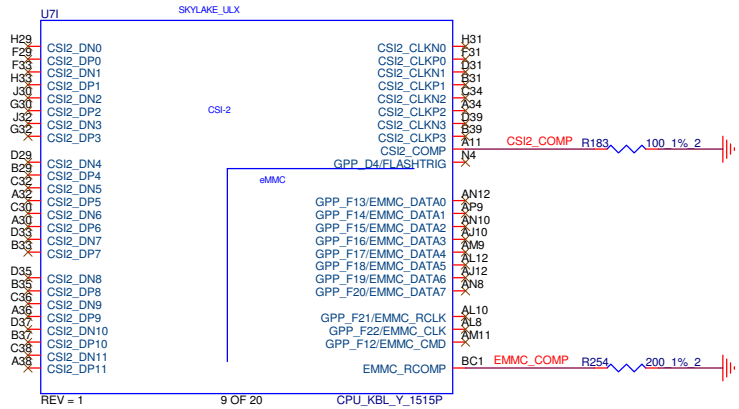
Date: Tuesday, January 23, 2018 Sheet 4 of 39



 Quanta Computer Inc. PROJECT : ZDJ	
Size	Document Number KBL-Y CPU (I2C/HDA/ID)
Date: Monday, January 22, 2018	Sheet 5 of 39



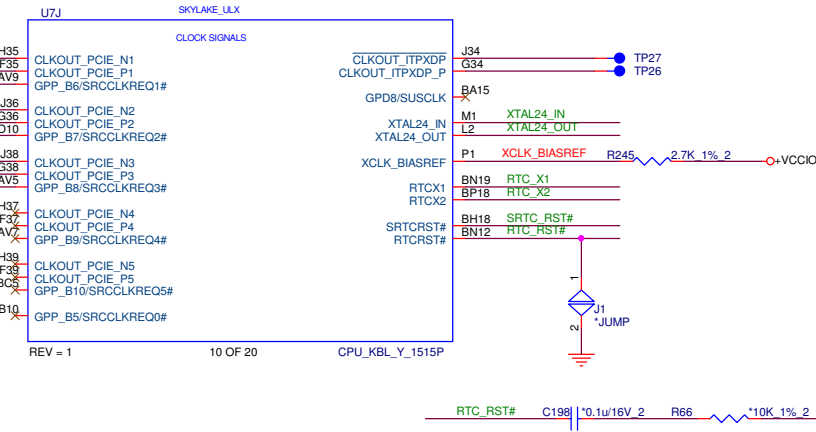
Function	Vendor P/N	SATAGP1 (OR gate)	Pin 1 (CONFIG_3)	Pin 69 (CONFIG_1)
SATA SSD	Liteon CV3-SD128 Liteon CV3-SD256 Liteon CV3-SD512	L	GND	GND
PCI-E SSD	Phison PS5008-E8	H	GND	NC(H)
PCI-E LTE	Fibocom L850-GL	H	NC(H)	GND



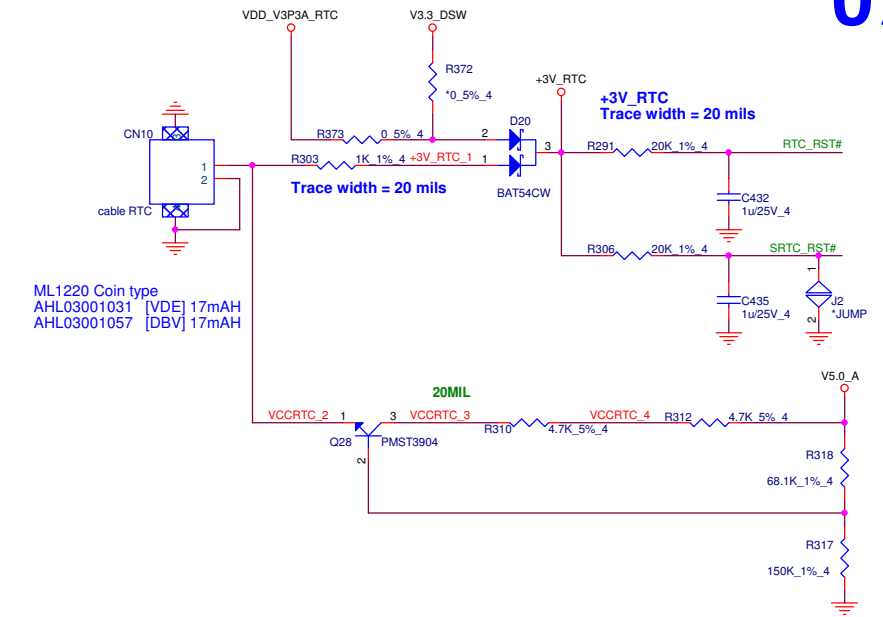
WLAN

LTE

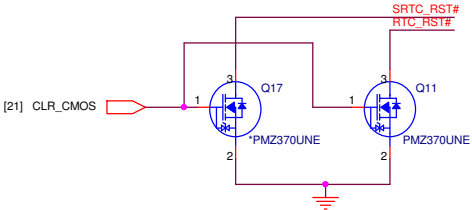
SSD



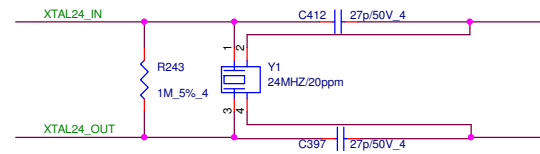
RTC Circuit (RTC)



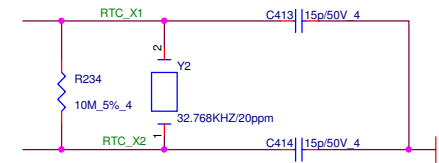
EC reset RTC

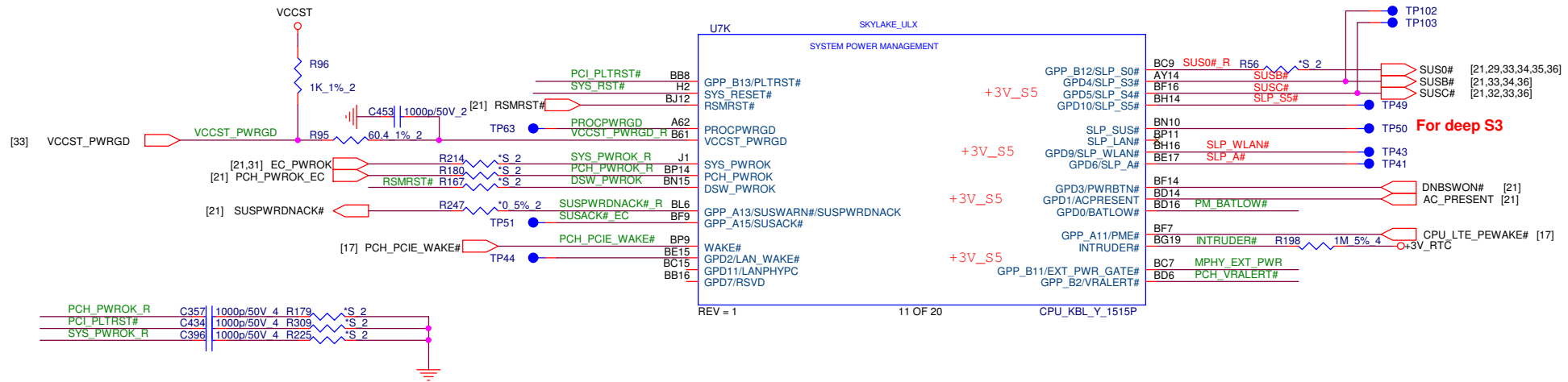


PCH XTAL-24MHz

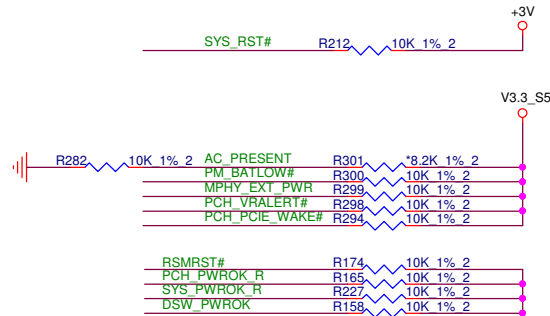
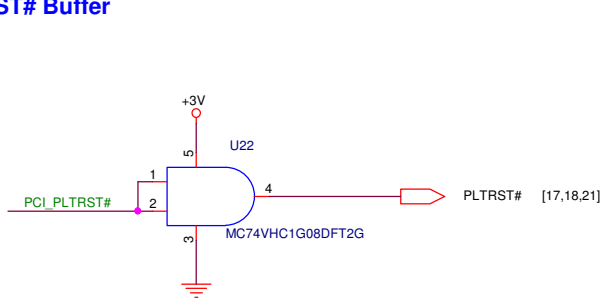


RTC XTAL-32.768KHz



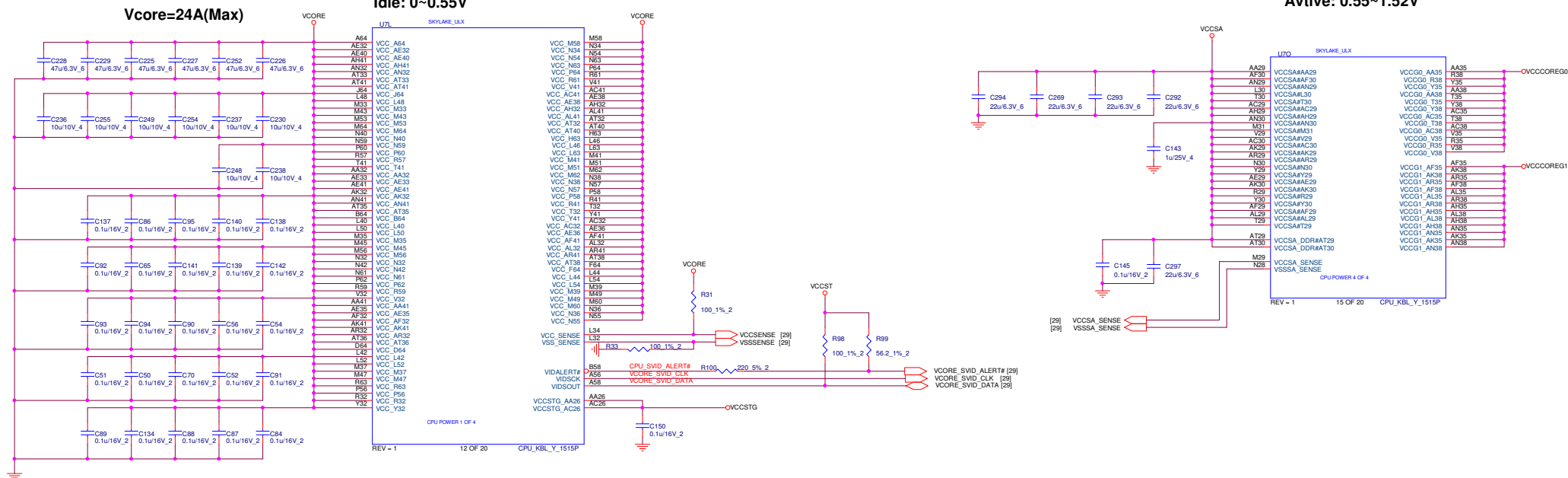


PLTRST# Buffer

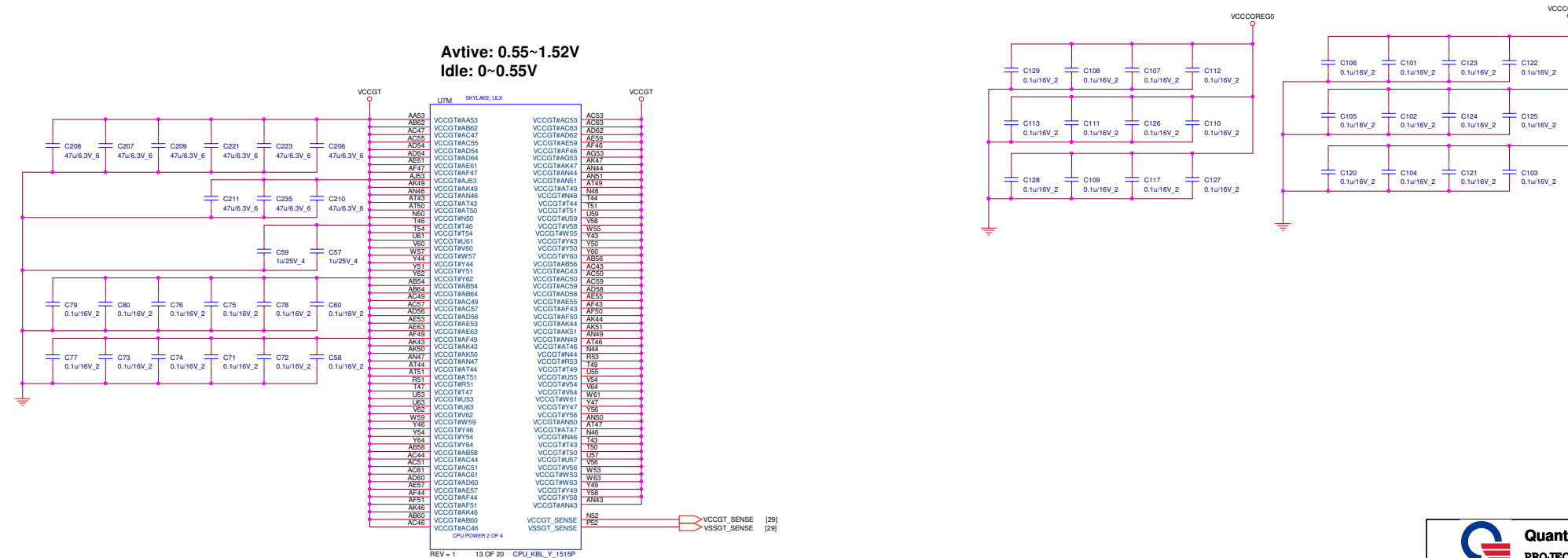


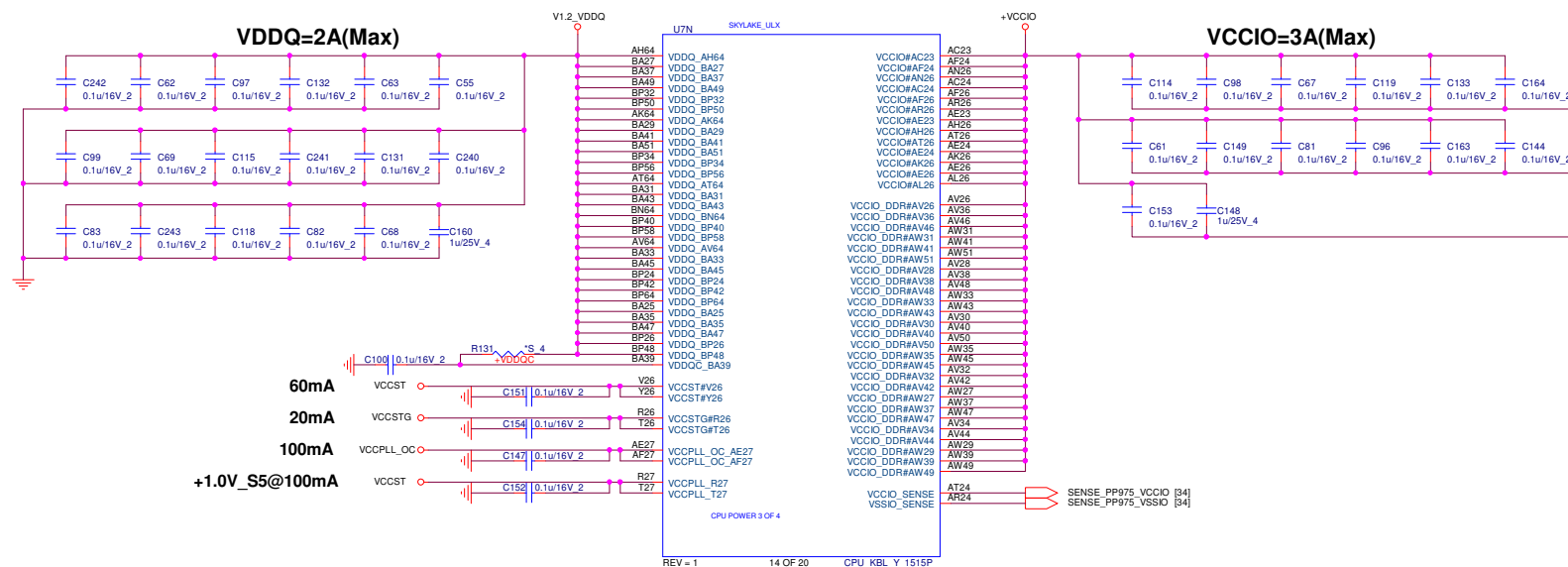
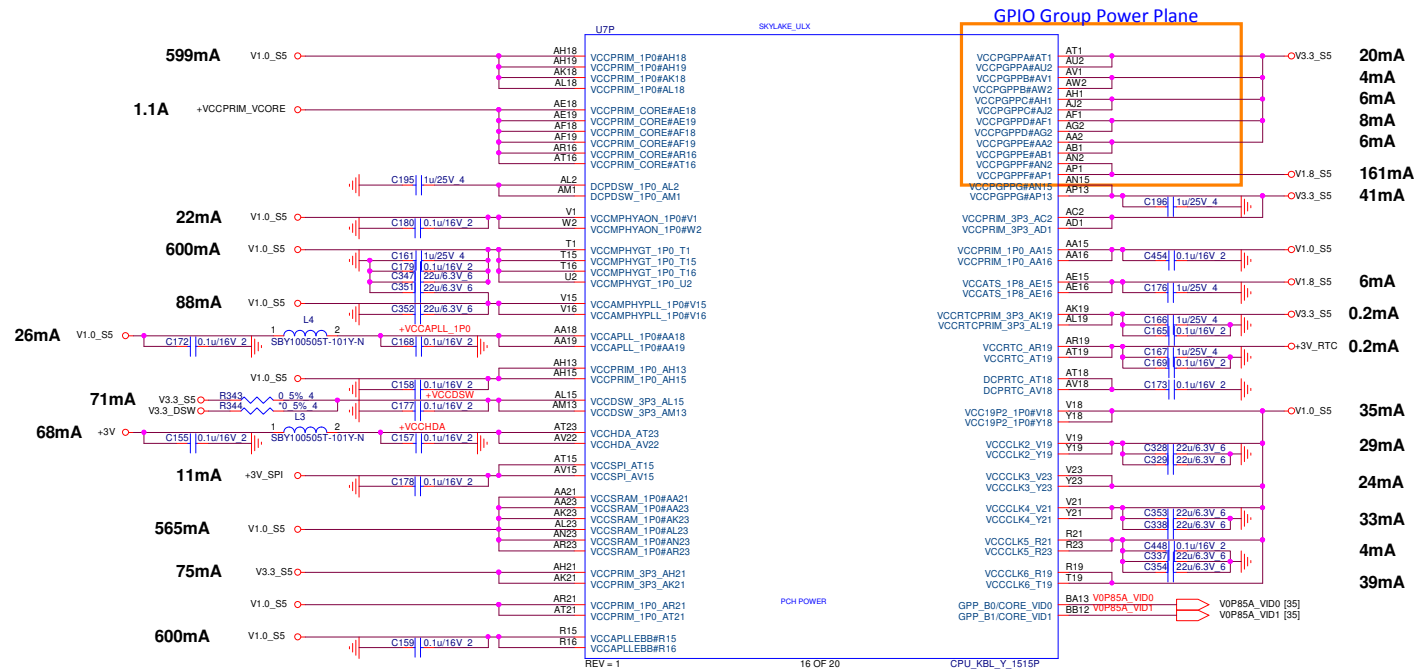
Active: 0.55~1.52V
Idle: 0~0.55V

Active: 0.55~1.52V



















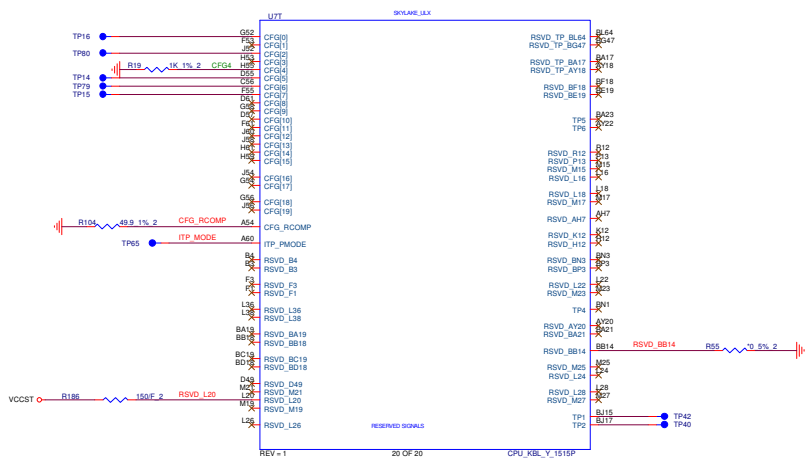
Active: 0.55~1.52V
Idle: 0~0.55V



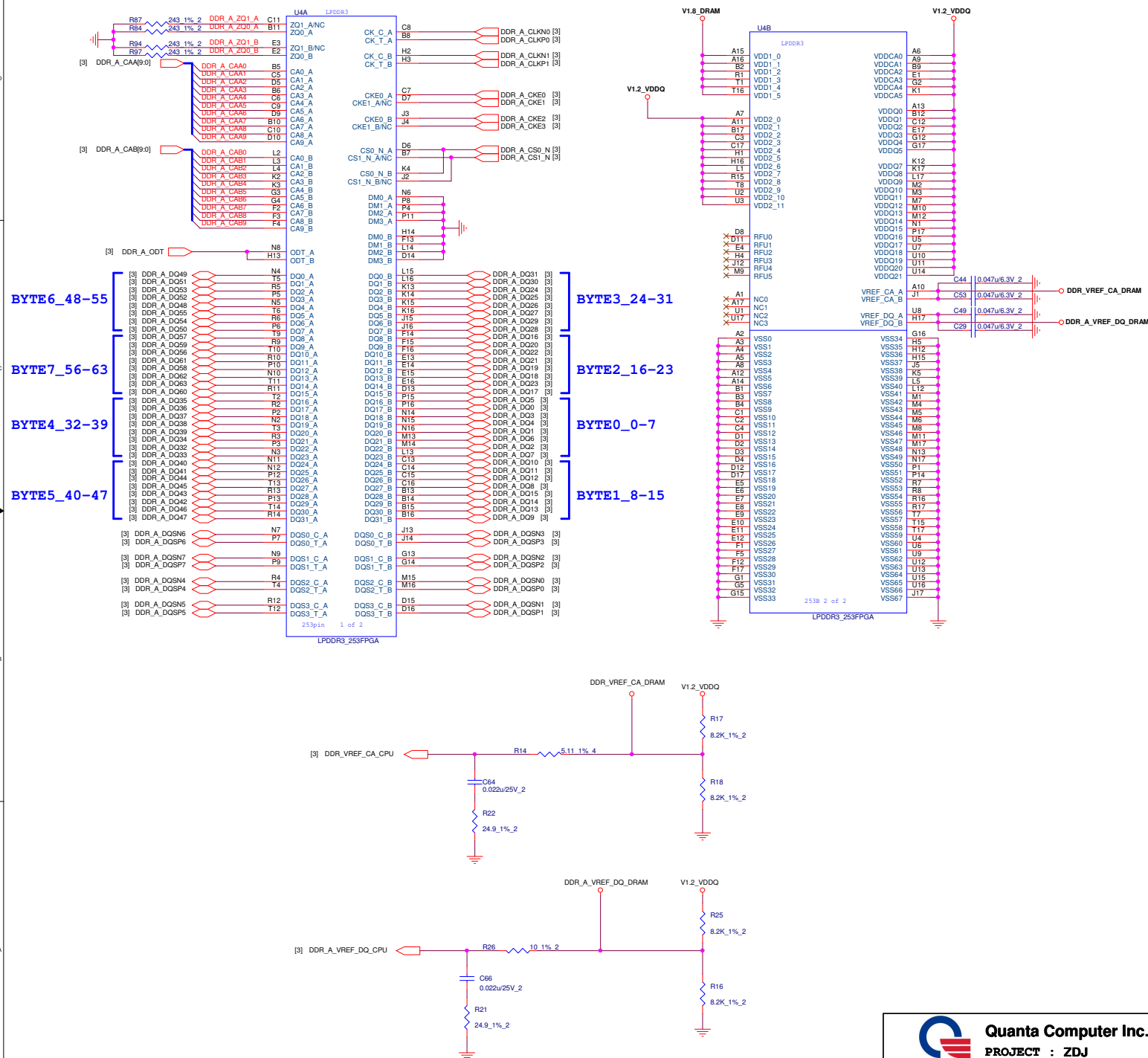


Processor Strapping

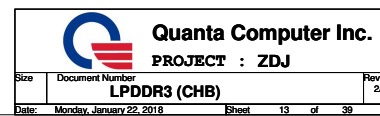
Pin Name	Strap description	Sampled	Configuration	note
GPP_B14 (SPKR)	Top-Block Swap override	PCH_PWROK	0 = "Disable Top Swap (IPD 20K) 1 = Enable Top Swap Mode	-3V  R291 10K 1% 2  AC2_SPK [B,19]
GPP_B18	No reboot	PCH_PWROK	0 = "Disable No Reboot (IPD 20K) 1 = Enable No Reboot Mode	-3V  R276 1K 1% 2  No_Reboot [5]
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSMRST#	0 = "Disable Intel ME Crypt to TLS(IPD 20K) 1 = Enable Intel ME Crypt to TLS	V3.3_SS  R258 10K 1% 2  SMBALERT# [4]
GPP_B22 (GSF1_MOSI)	Boot BIOS Strap Bit (BBS)	PCH_PWROK	0 = "SPI (IPD 20K) 1 = LPC	-3V  R279 1K 1% 2  GSF1_MOSI [5]
GPP_C5 (SML0ALERT#)	eSPI or LPC	RSMRST#	0 = "LPC is selected for EC (IPD 20K) 1 = eSPI selected for EC	V3.3_SS  R257 1K 1% 2  SML0ALERT# [4]
SPI0_MOSI	Reserved	RSMRST#	(IPU 15 - 40K)	
SPI0_MISO	Reserved	RSMRST#	(IPU 15 - 40K)	
GPP_B23 (SML1ALERT# /PCHHOT#)	Reserved	RSMRST#	(IPD 20K)	
SPI0_I02	Reserved	RSMRST#	(IPU 15 - 40K)	
SPI0_I03	Reserved	RSMRST#	(IPU 15 - 40K)	
HDA_SDO / I2S_TXDO	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = "Enable security in the Flash Descriptor (IPD 20K) 1 = Disable Flash Descriptor Security (Override)	change location to near CPU to prevent impact HDA_SDO signal [21] ME_WIR  R252 1K 1% 2  HDA_SDO_U_T [8]
GPP_E19 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	0 = "Port B is not detected (IPD 20K) 1 = Port B is detected	V3.3_SS  R202 2.2K 5% 2  DDPB_CTRLDATA [2]
GPP_E21 (DDPC_CTRLDATA)	Display Port C Detected	PCH_PWROK	0 = "Port C is not detected (IPD 20K) 1 = Port C is detected	V3.3_SS  R213 2.2K 5% 2  DDPC_CTRLDATA [2]



12

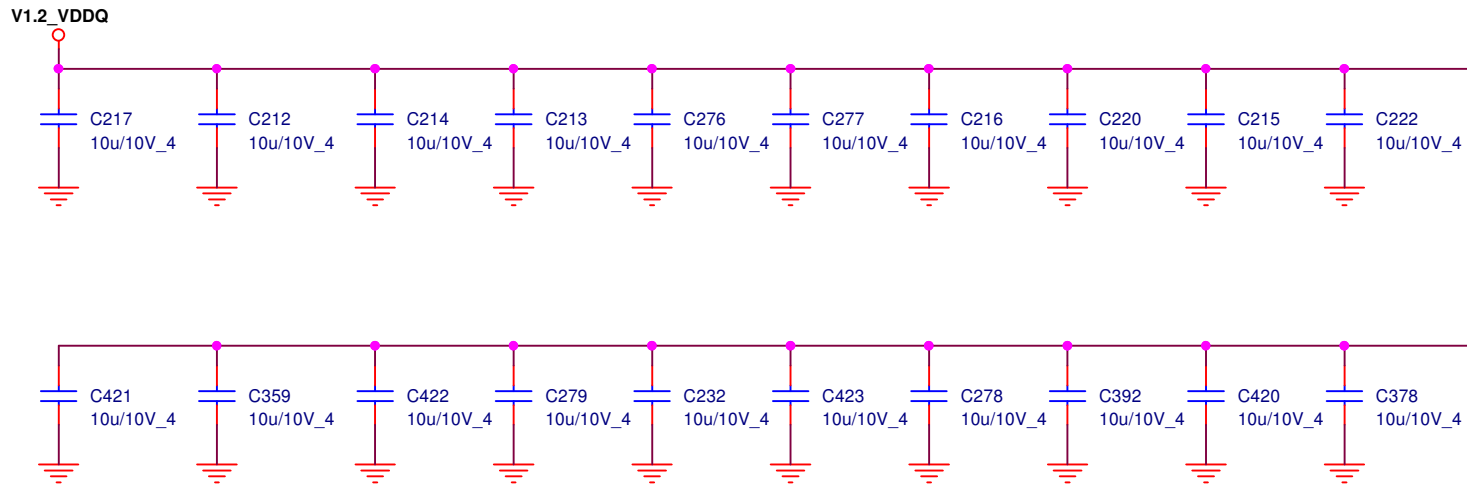


13

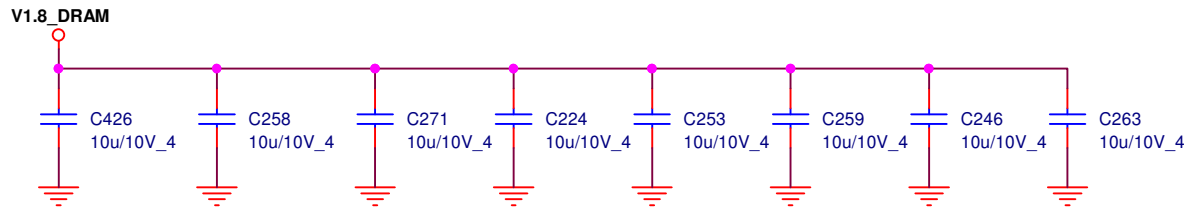


DE-CAPS FOR MEMORY CHANNEL A/B

VDDQ/VDD2/VDDCA DECOUPLING



VDD1 DECOUPLING



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PROJECT : ZDJ

Size

Document Number

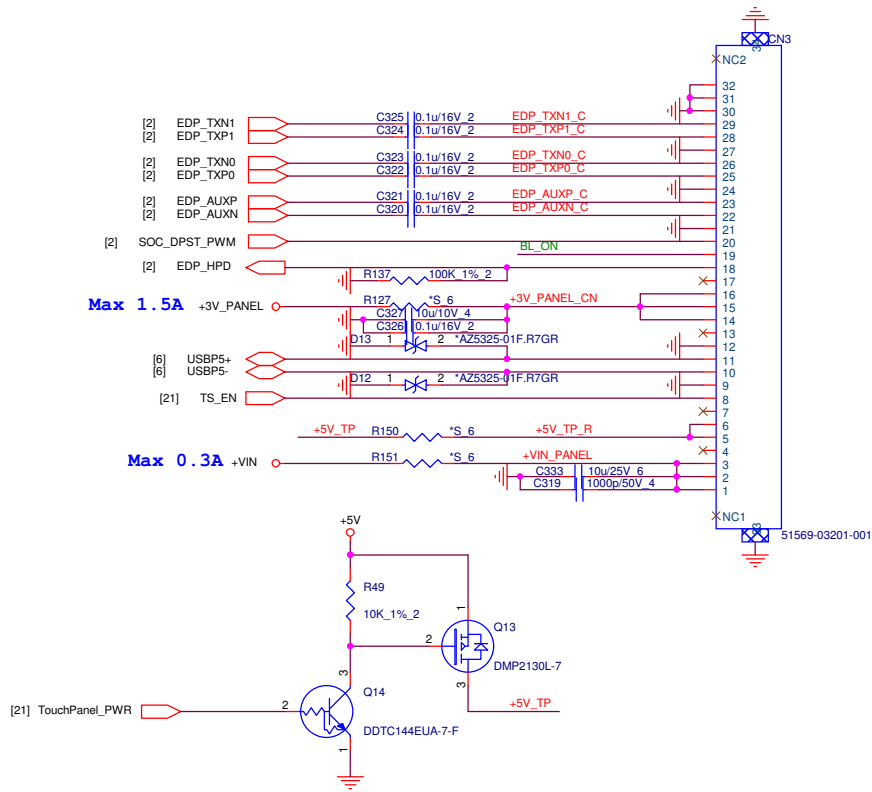
LPDDR3 DE-CAP

Rev
2A

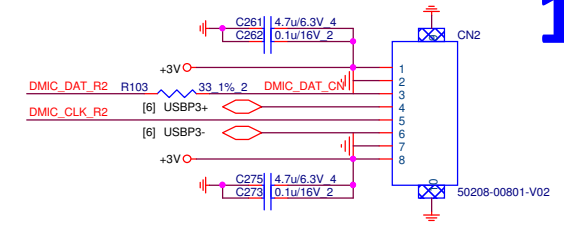
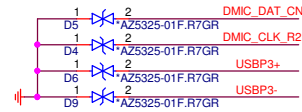
Date: Monday, January 22, 2018

Sheet 14 of 39

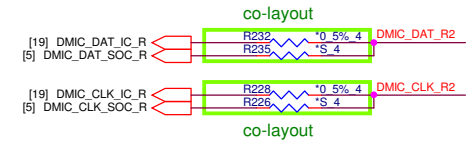
eDP Connector (LDS)



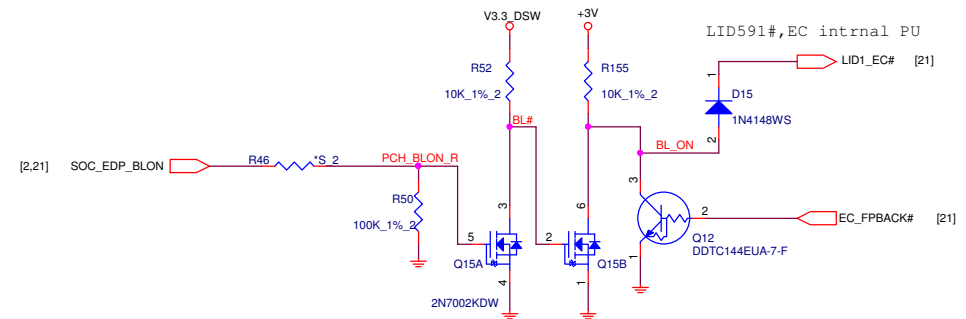
CCD+DMIC (FCM)



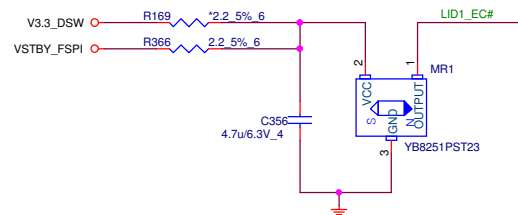
15

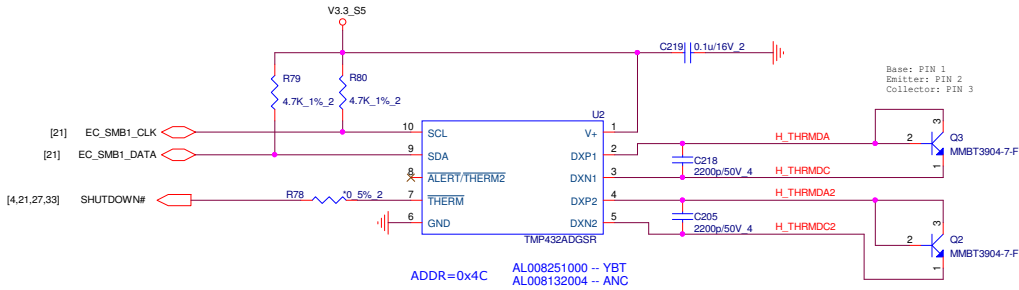


Backlight Control (LDS)

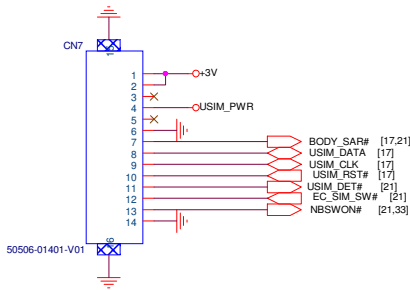


Hall Sensor (HSR)

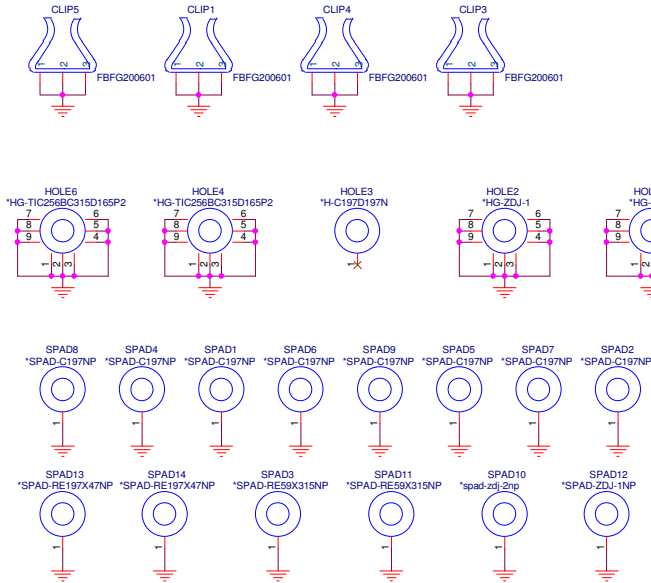


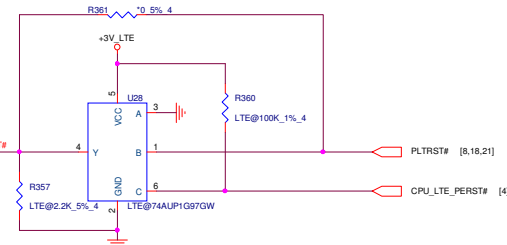


Daughter Board

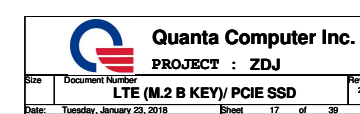


HOLE(OTH)

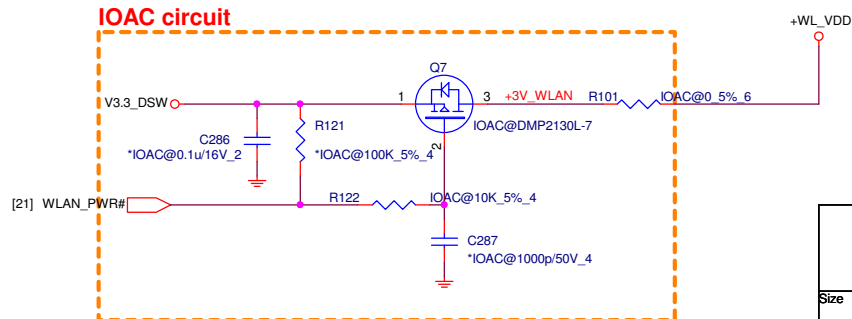




PCIE SSD-BGA 1260 TYPE (HDD)

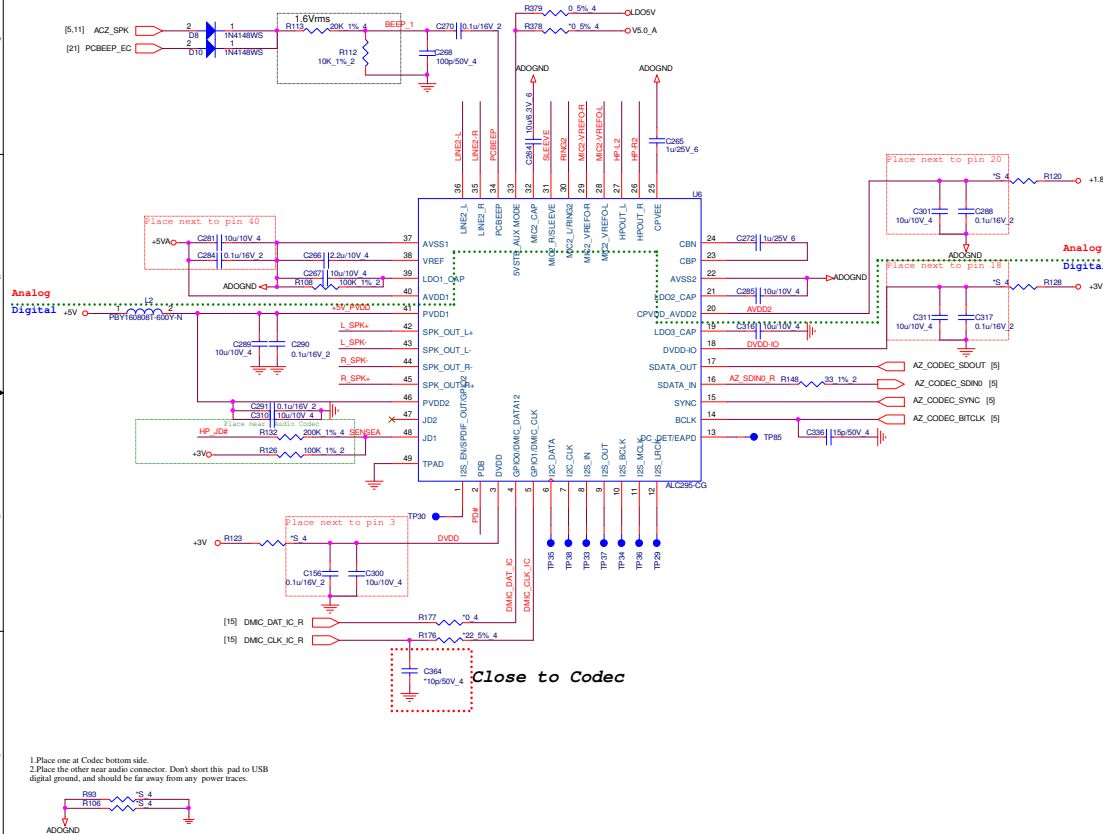


18

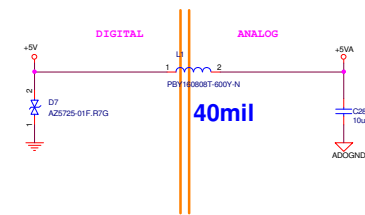


Codec ALC295 (ADO)

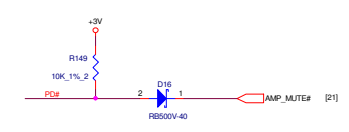
trace width of SLEEVE & RING2
are required at least 40mil and
its length should be as short as possible



Codec PWR 5V(ADO)

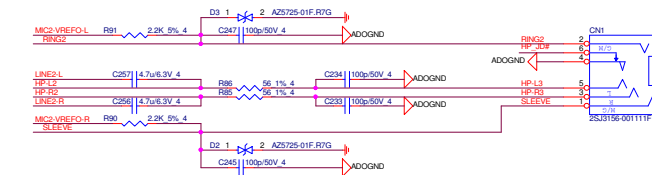


Mute(ADO)

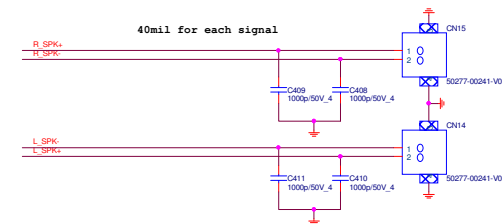


19

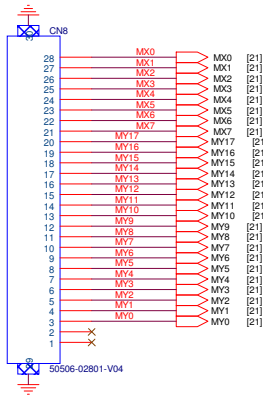
Universal Audio Jack (ADO)



Internal Speaker (ADO)

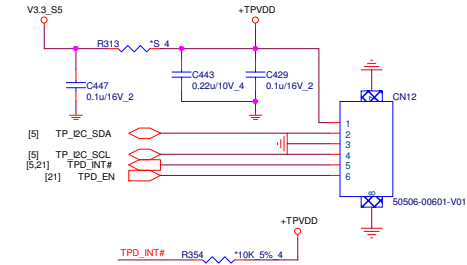


Keyboard conn (KBC)

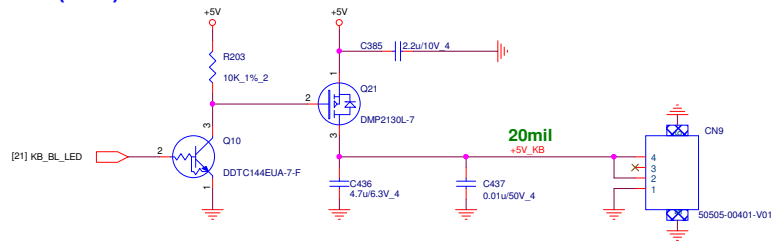


TOUCHPAD (TPD)

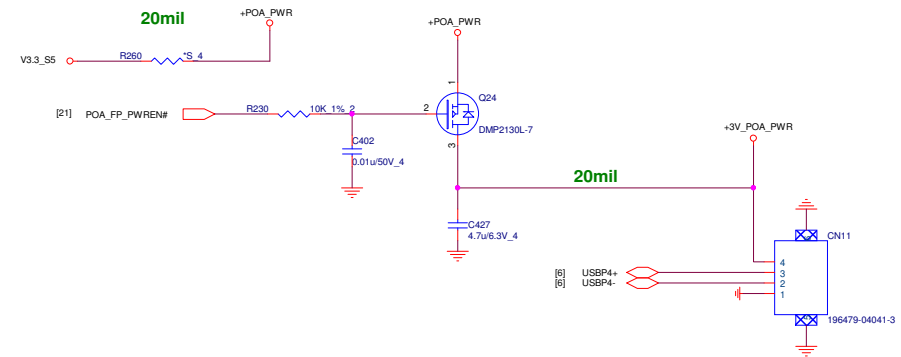
TPD->100kHz, TS=400KHz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u TS=3x5inch
400kHz10-100u =2.4-0.4k.
100kHz 10-100u=9k-1k.



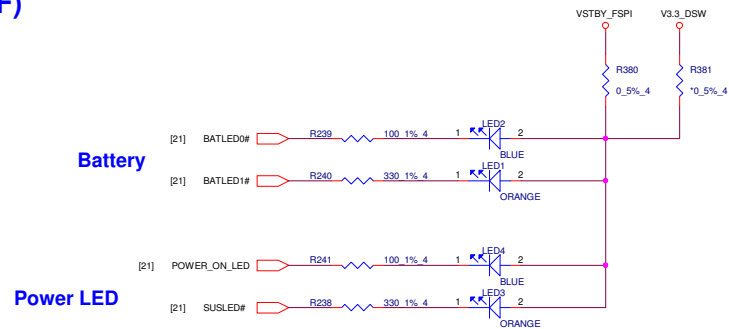
KB_BL LED (KBC)



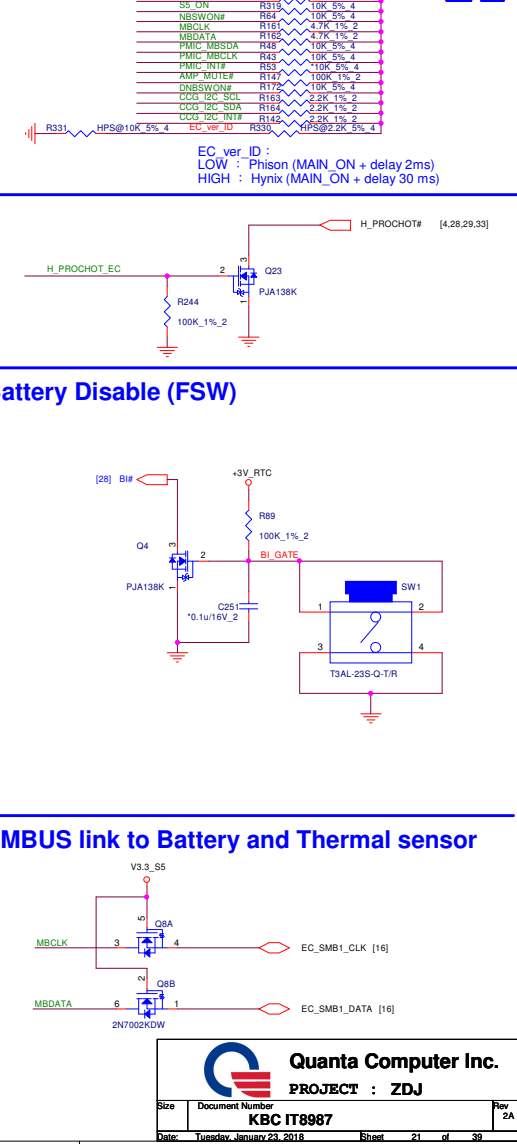
POA Fingerprint (FPD)

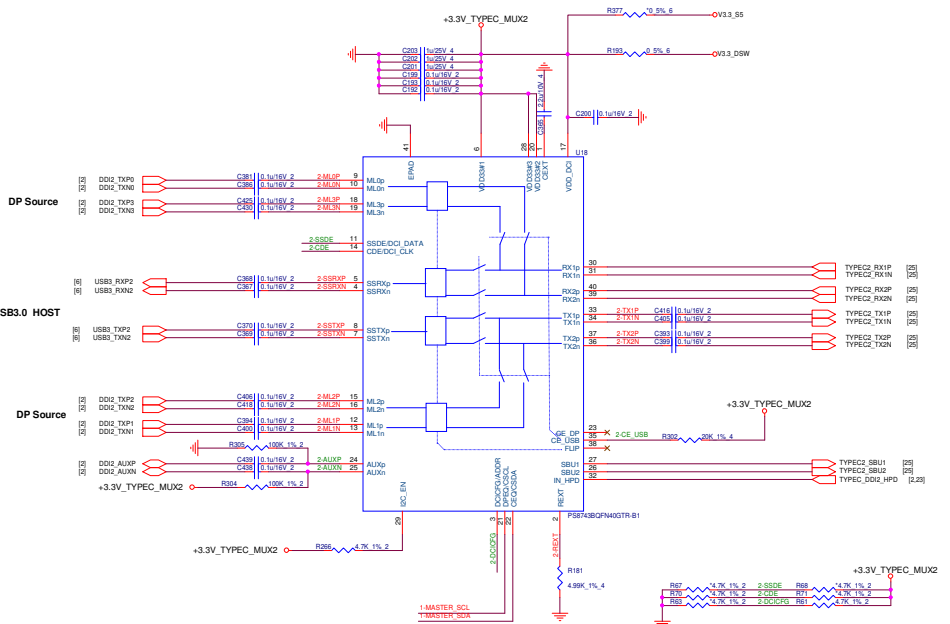


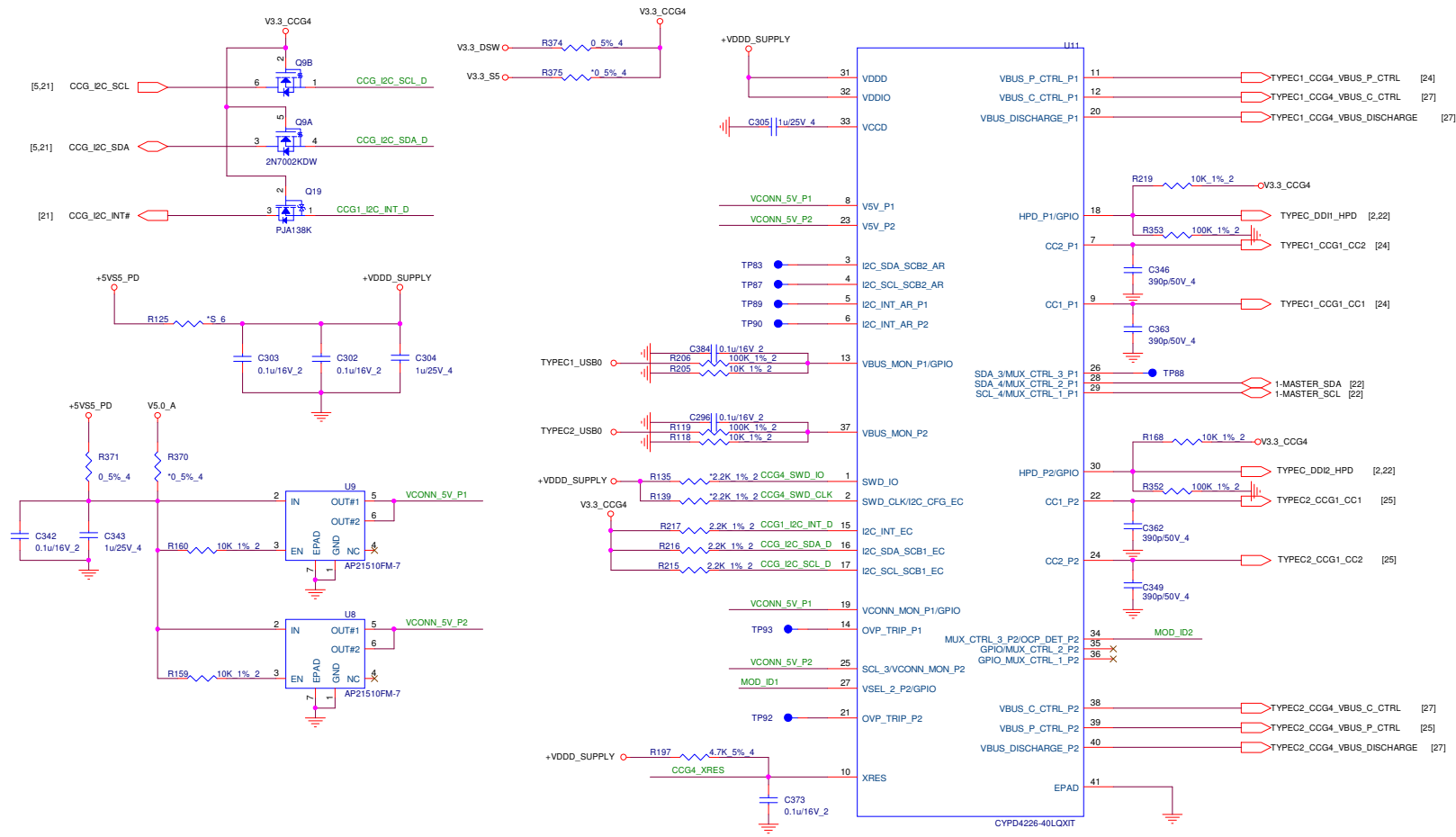
LED (UIF)



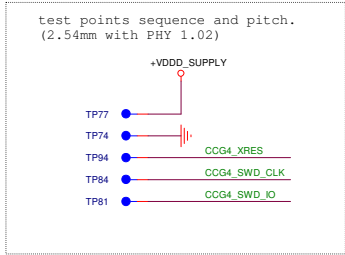
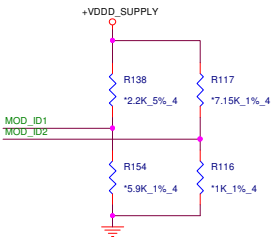
21



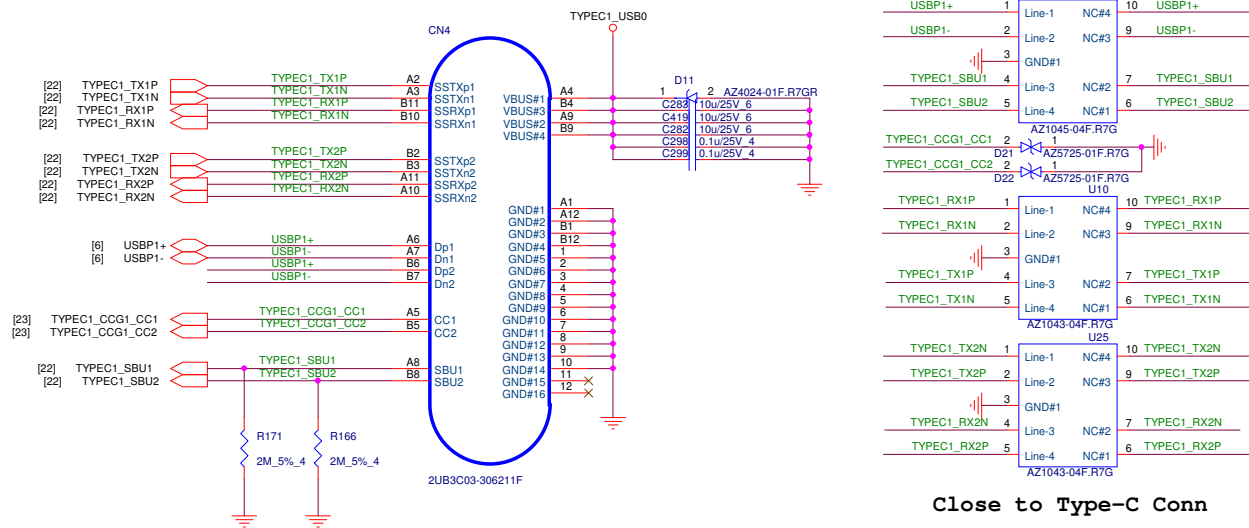
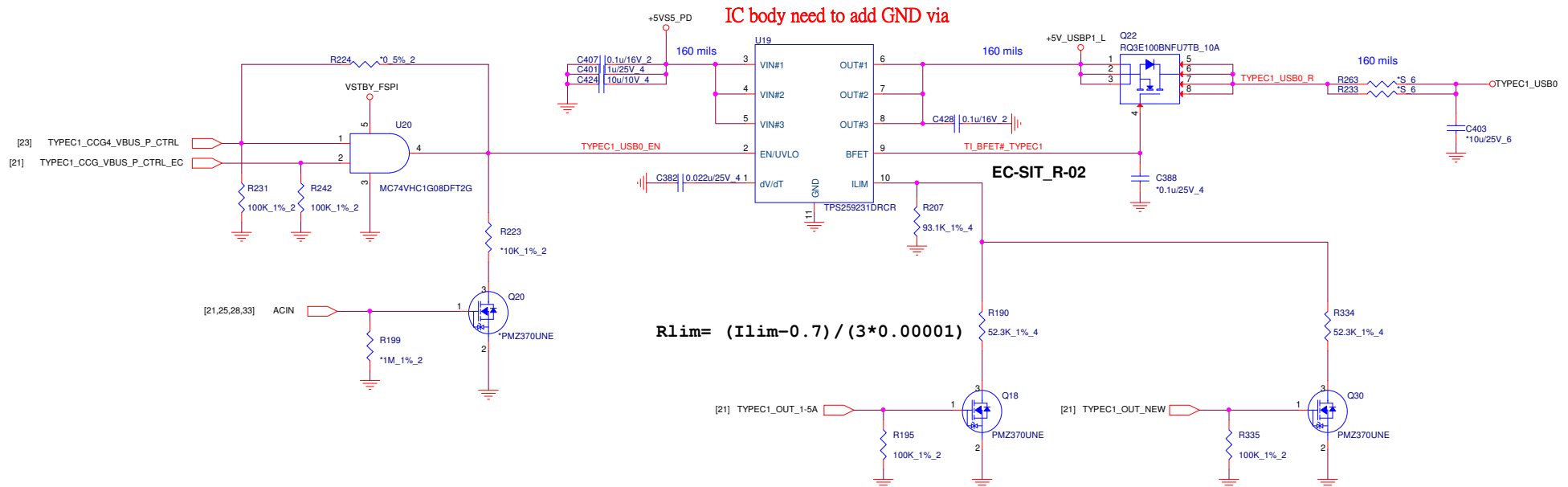




MOD_ID	Pull high	Pull down
L0	None	1K
L1	7.1K	1K
L5	3.09K	5.1K
L6	2.2K	5.9K



USB TYPE-C PORT1 (UB3)



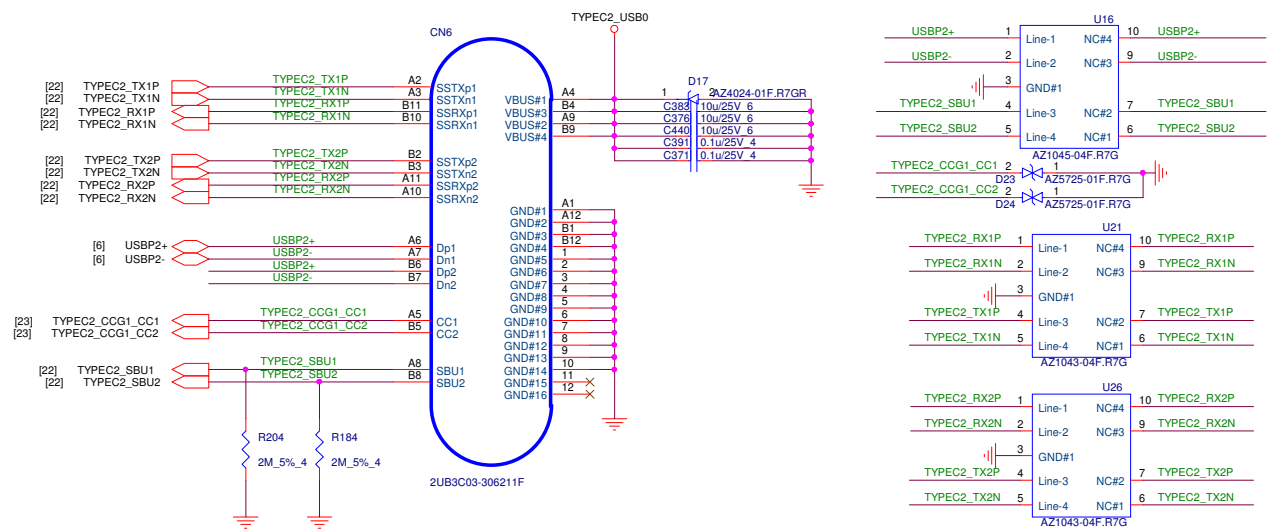
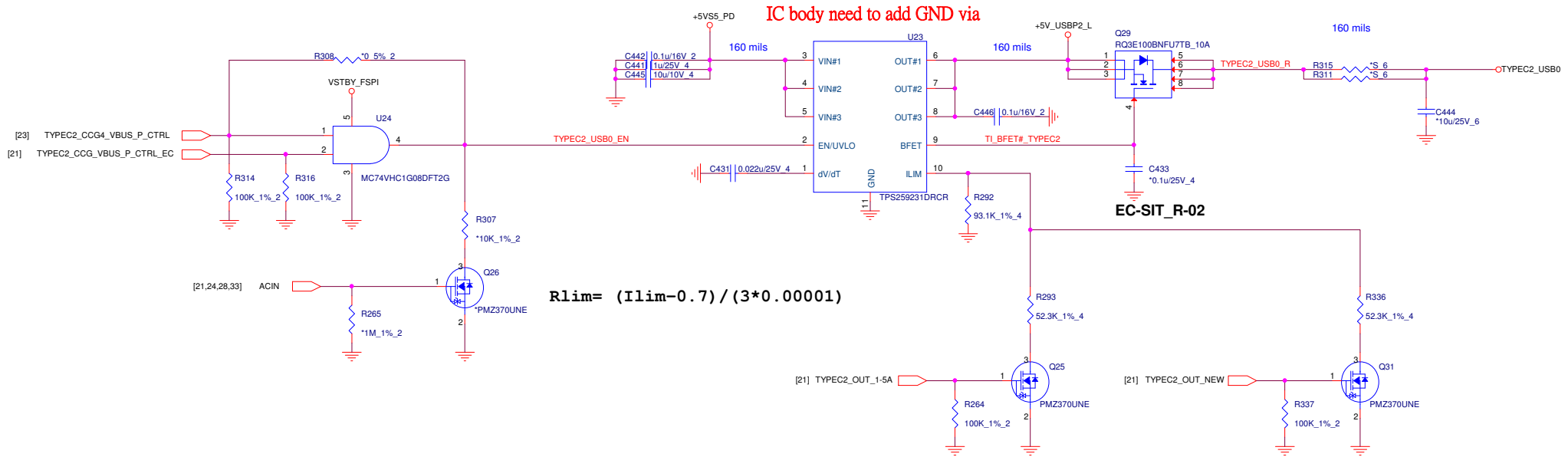
Close to Type-C Conn



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PROJECT : ZDJ

USB TYPE-C_1_PD+DP

Size	Document Number USB TYPE-C_1_PD+DP	Rev 2A
Date:	Monday, January 22, 2018	Sheet 24 of 39



Close to Type-C Conn

Quanta Computer Inc.

PROJECT : ZDJ

Size	Document Number	Rev	2A
USB TYPE-C_2_PD+DP			
Date: Monday, January 22, 2018		Sheet	25 of 39

[17] V1.8_DRAM
+0.9V_SSD
LDO3V
V3.3_DSW

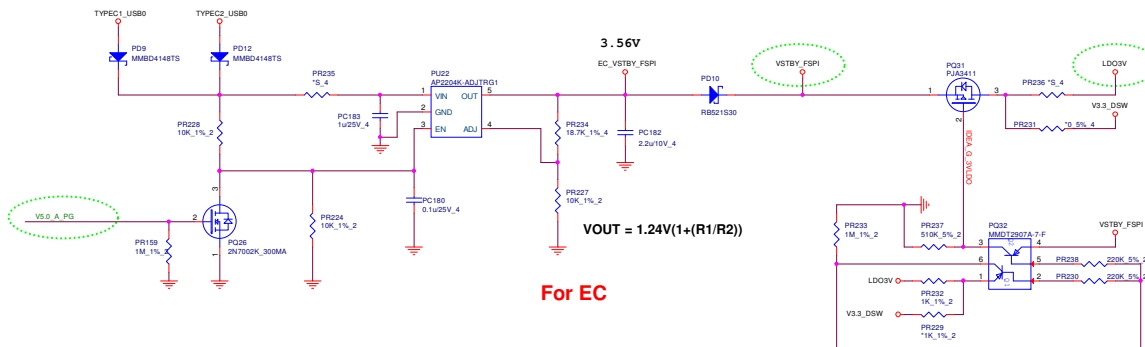
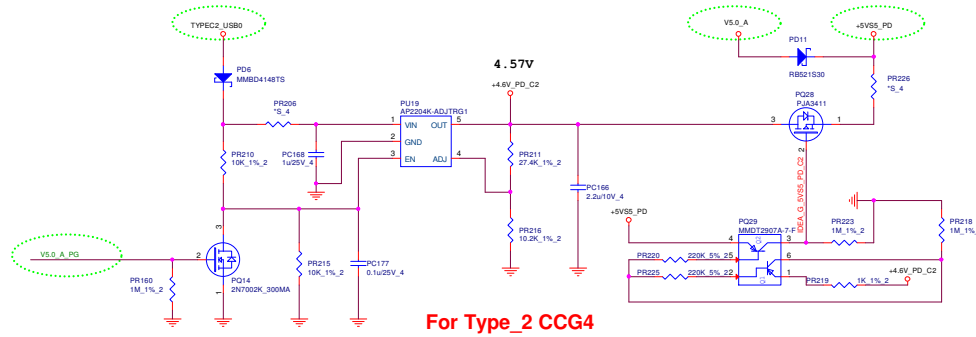
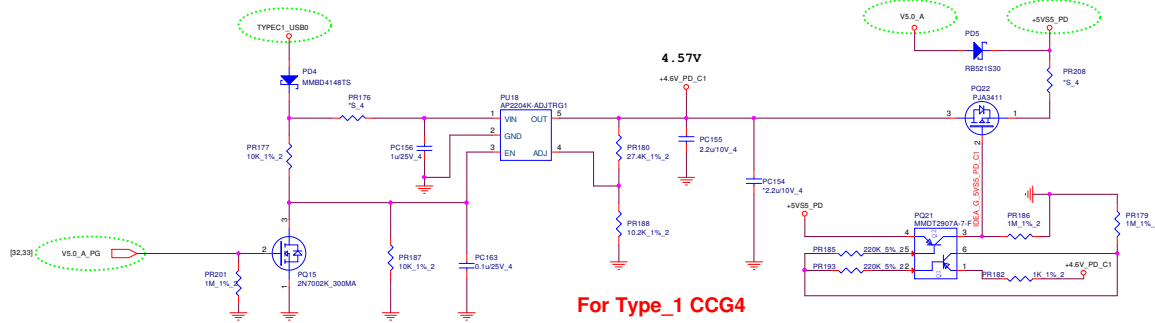
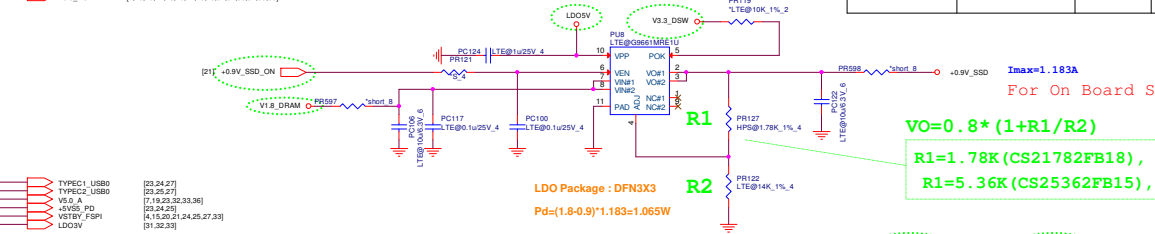
[12,13,14,33,36]
[19,31,32,33,36]
[7,10,15,17,18,20,22,23,28,31,32,33,34,35,36]

TYPEC1_USB0
TYPEC2_USB0
V5.0_A
+5VSS_PD
VSTBY_FSP1
LDO3V

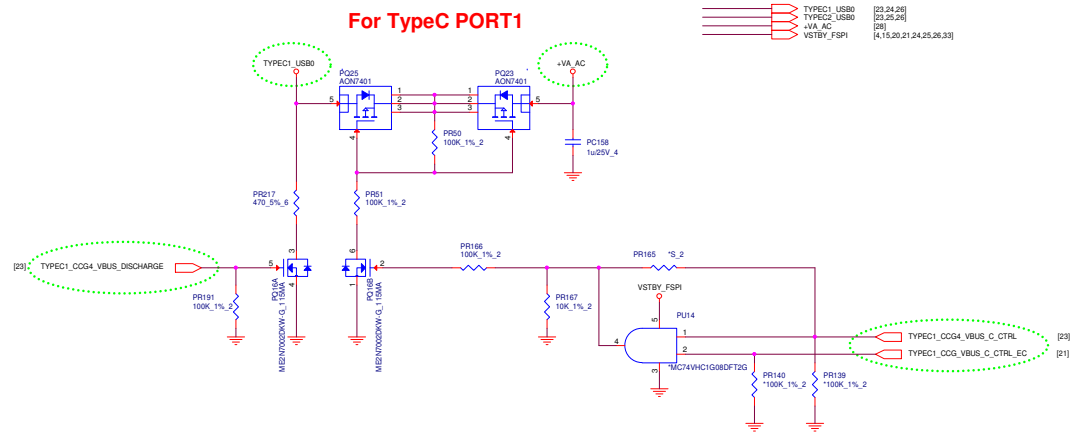
[23,24,27]
[23,25,27]
[7,19,23,32,33,36]
[23,24,25]
[4,15,20,21,24,25,27,33]
[31,32,33]

Device	Net	A	Voltage
SSD (on board)	+0.9V_SSD (Hynix) +1.1V_SSD (Phison)	1.183A	+0.9V / +1.1V (total 1.183A)

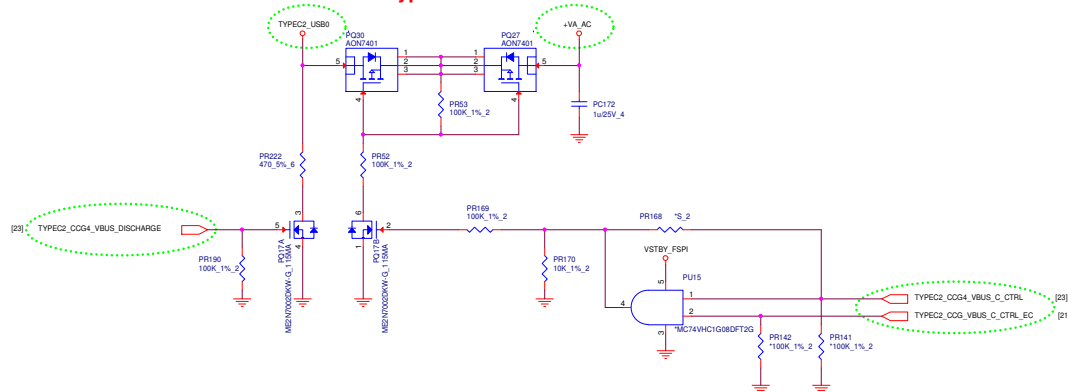
26



For TypeC PORT1

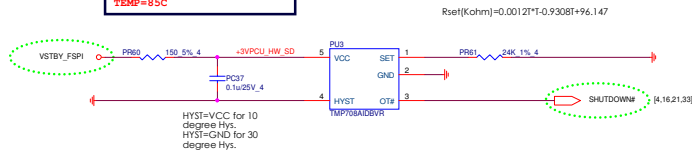


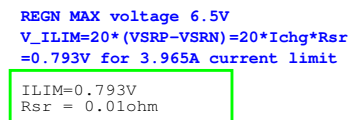
For TypeC PORT2

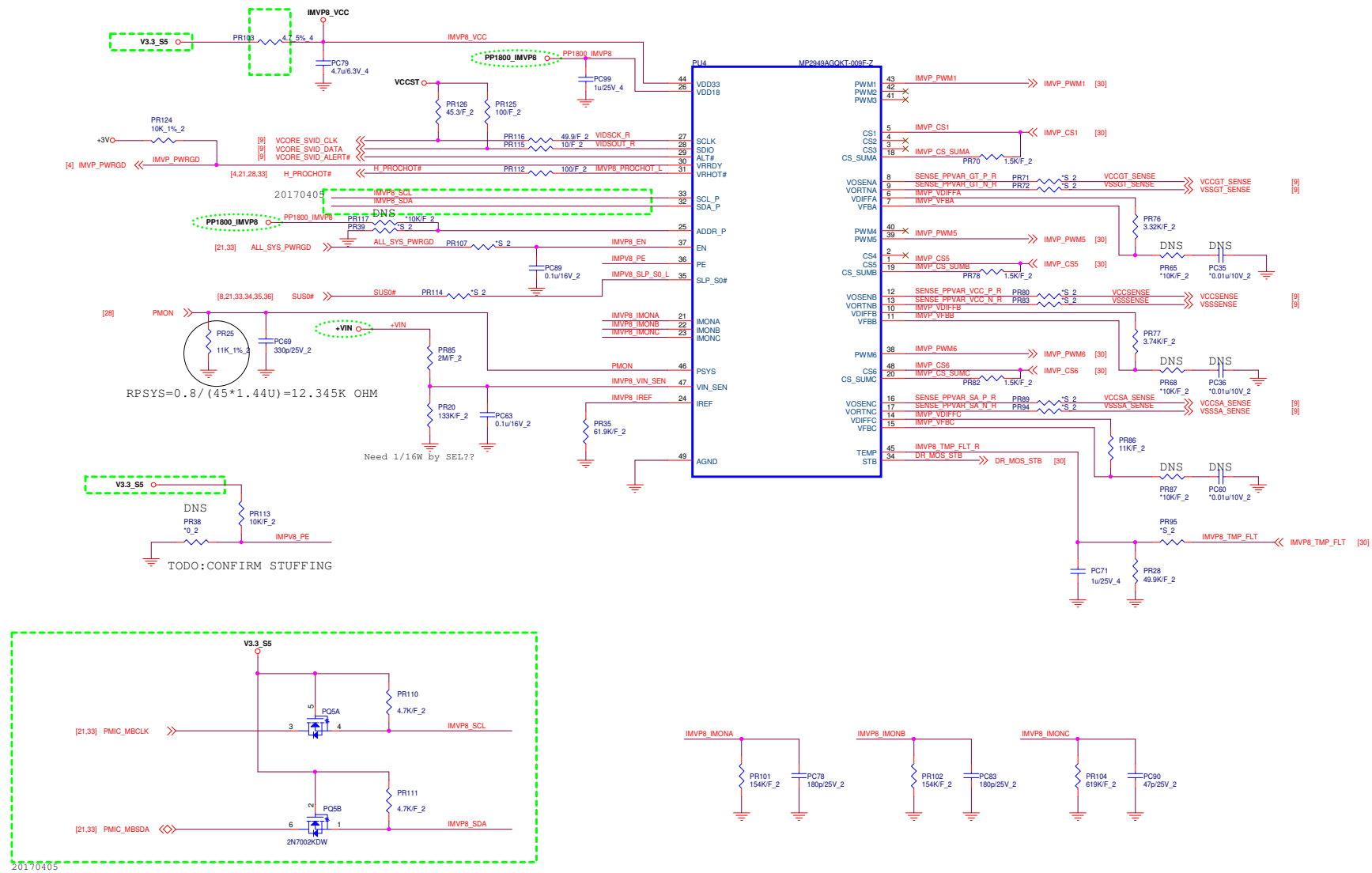


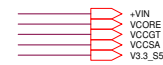
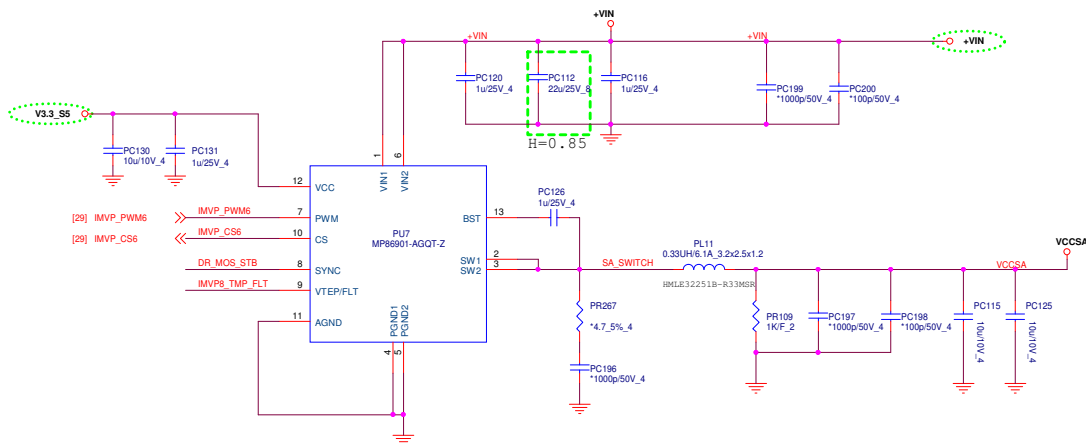
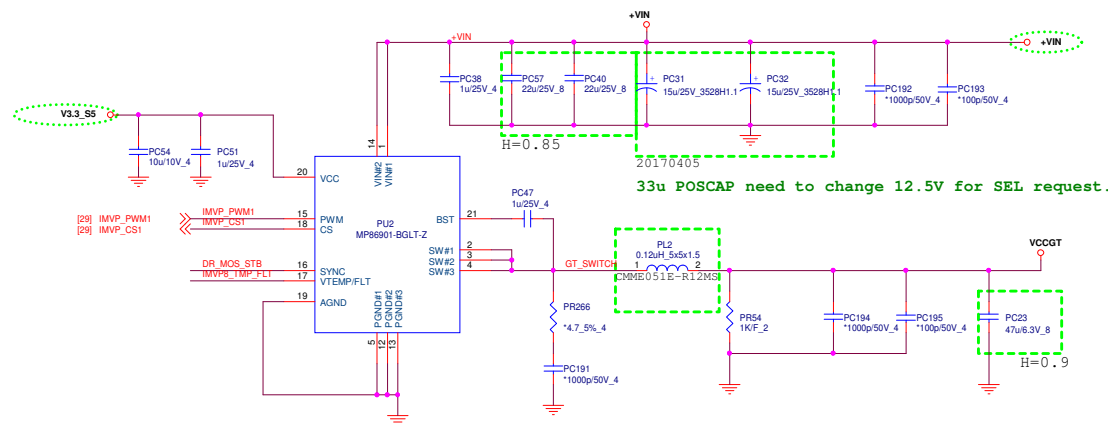
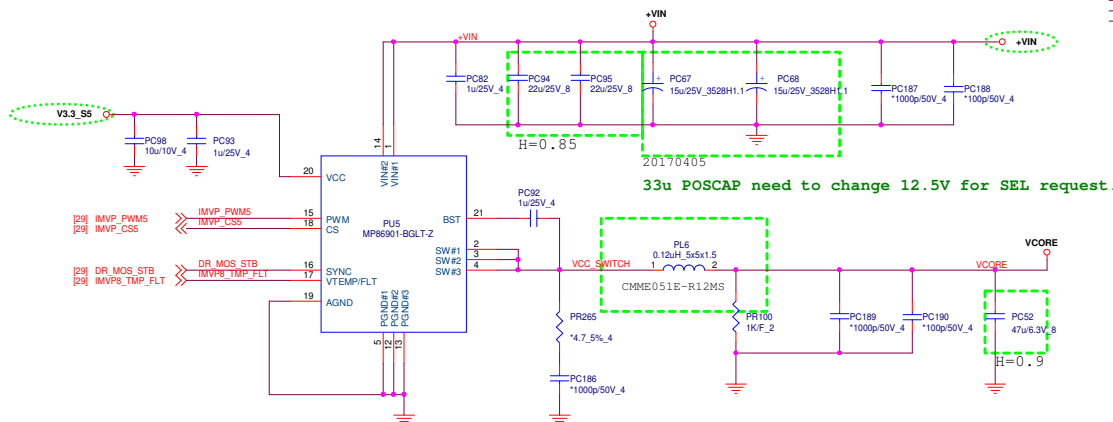
Thermal protection

For thermal protect point
Note placement position
TEMP=85C

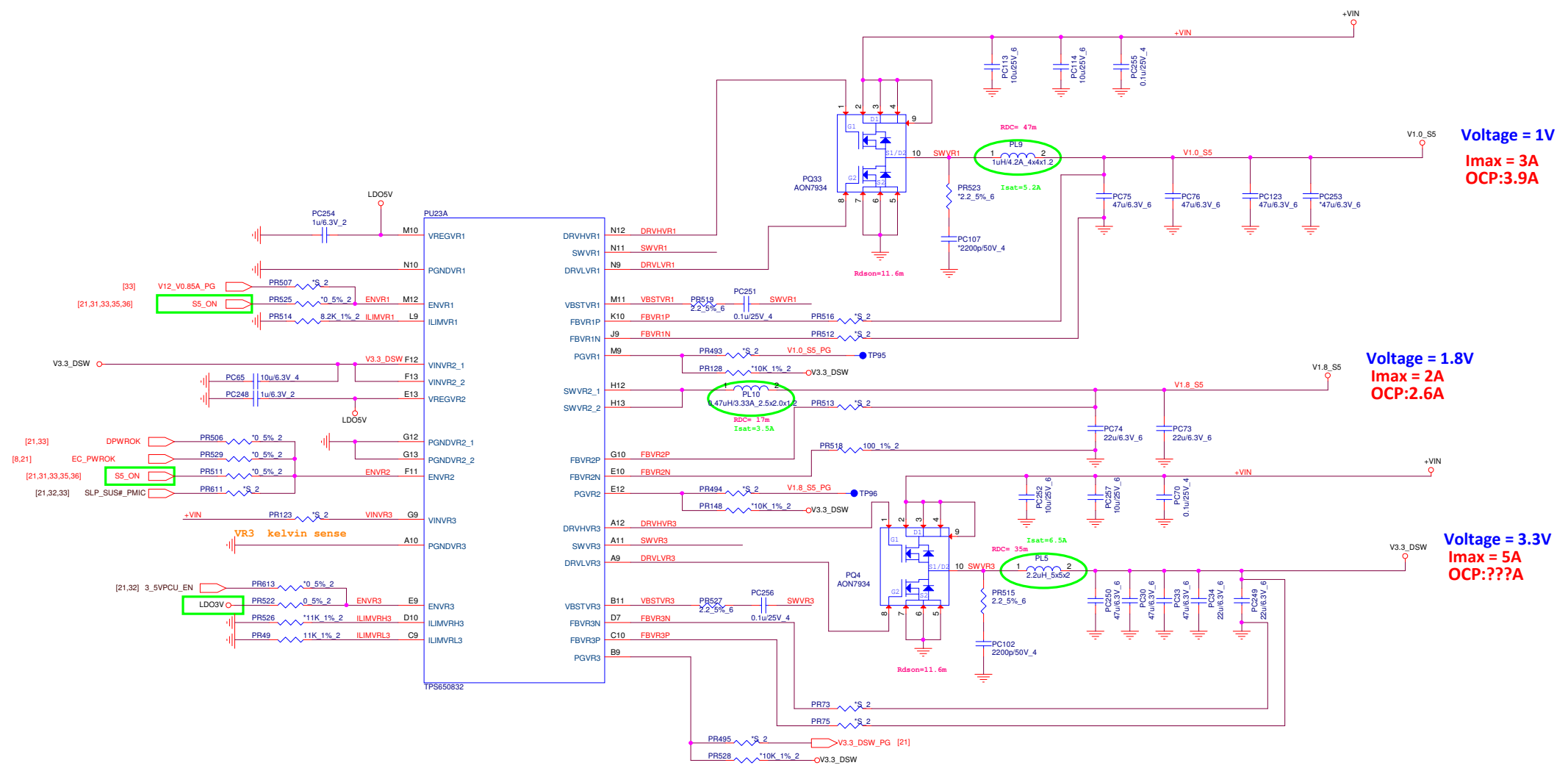








[15,28,29,31,32,33,34,35]
 [9]
 [9]
 [9]
 [4,5,6,8,10,11,16,20,21,22,23,29,33,36]



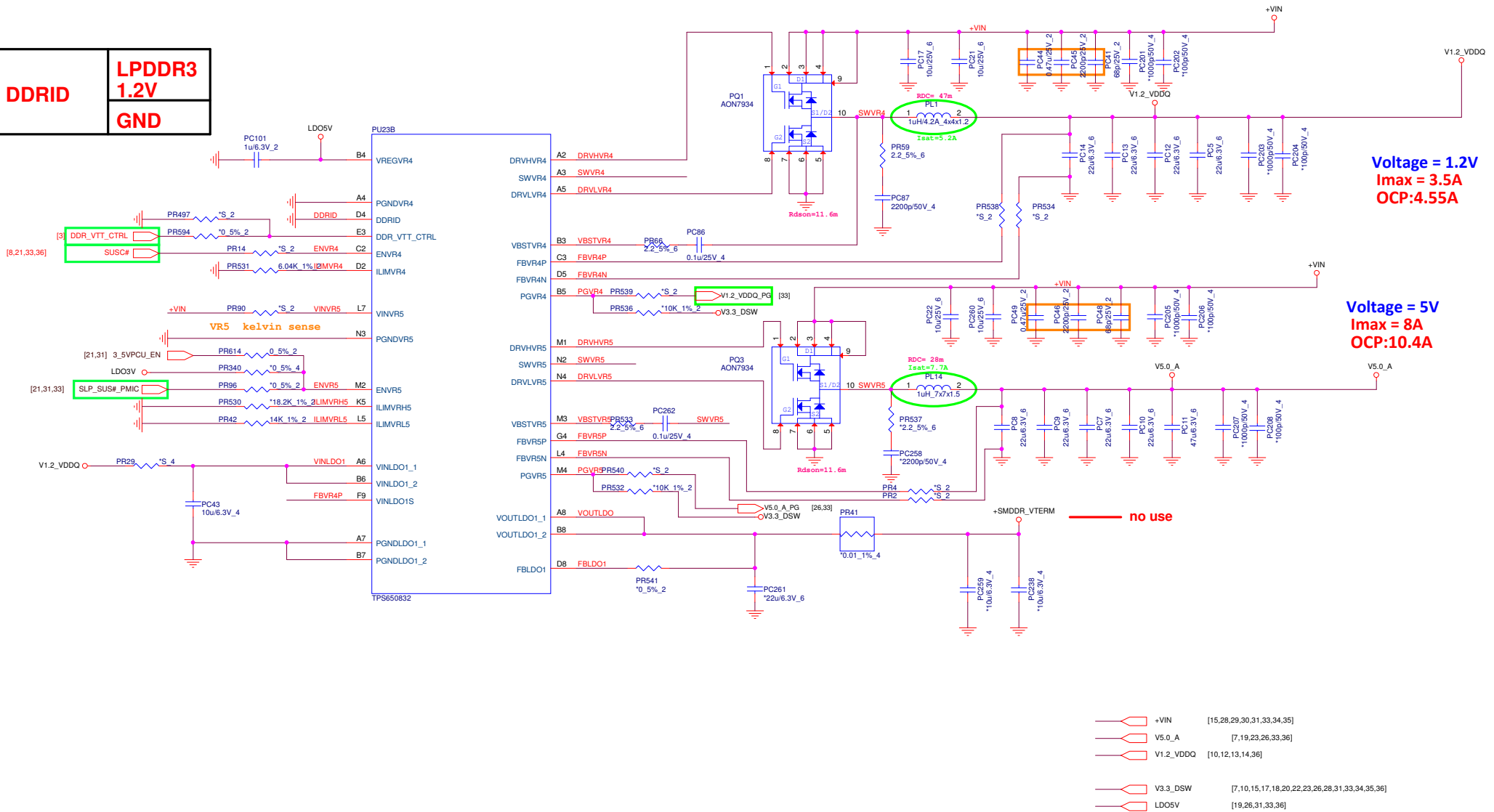
Voltage = 1V
I_{max} = 3A
OCP:3.9A

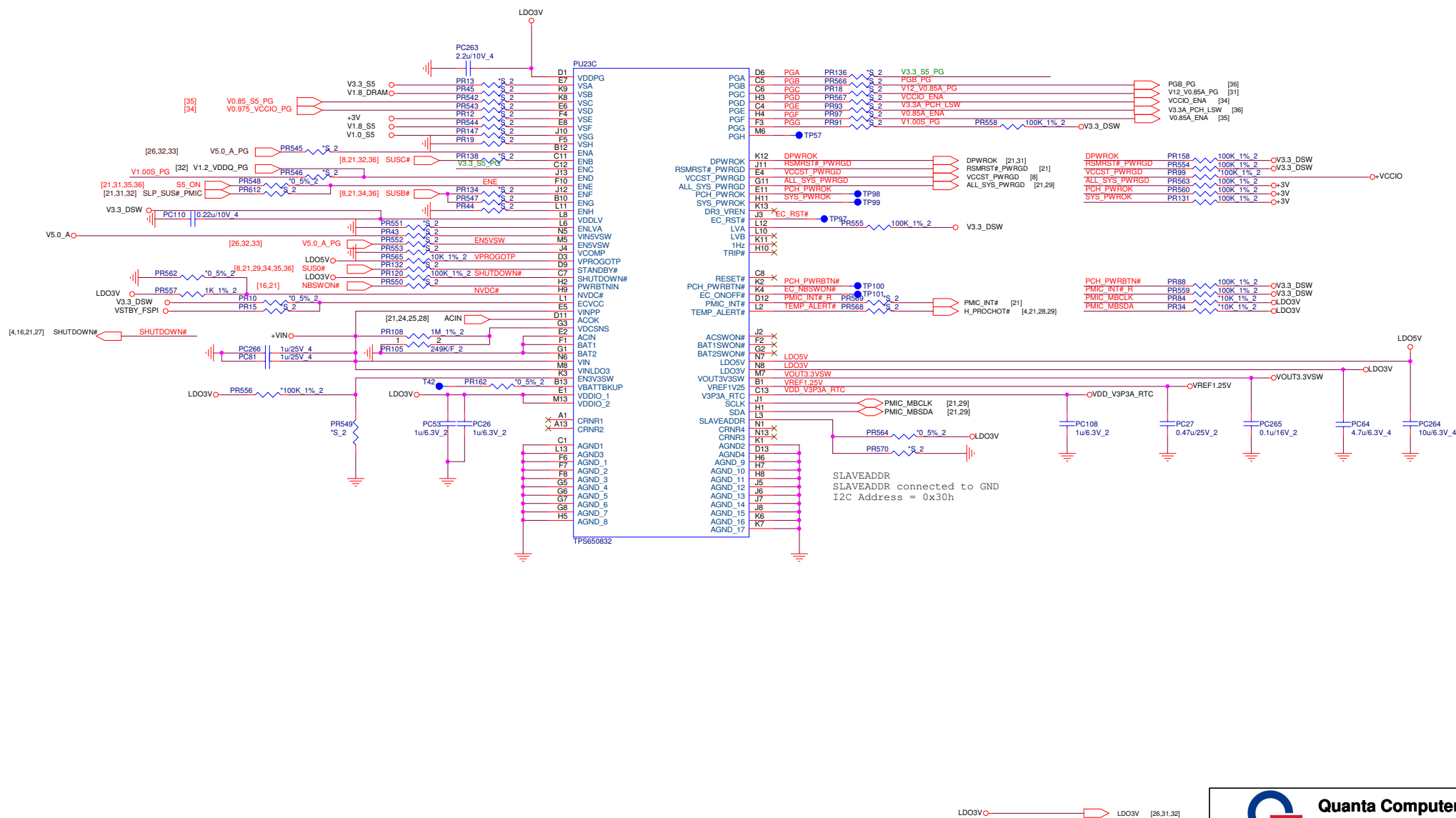
Voltage = 1.8V
I_{max} = 2A
OCP:2.6A

Voltage = 3.3V
I_{max} = 5A
OCP:???A

- +VIN [15,28,29,30,32,33,34,35]
- V1.0_S5 [10,33,36]
- V1.8_S5 [10,33,36]
- V3.3_DSW [7,10,15,17,18,20,22,23,26,28,32,33,34,35,36]
- LDO5V [19,26,32,33,36]
- LDO3V [26,32,33]

DDRID	LPDDR3
	1.2V
	GND

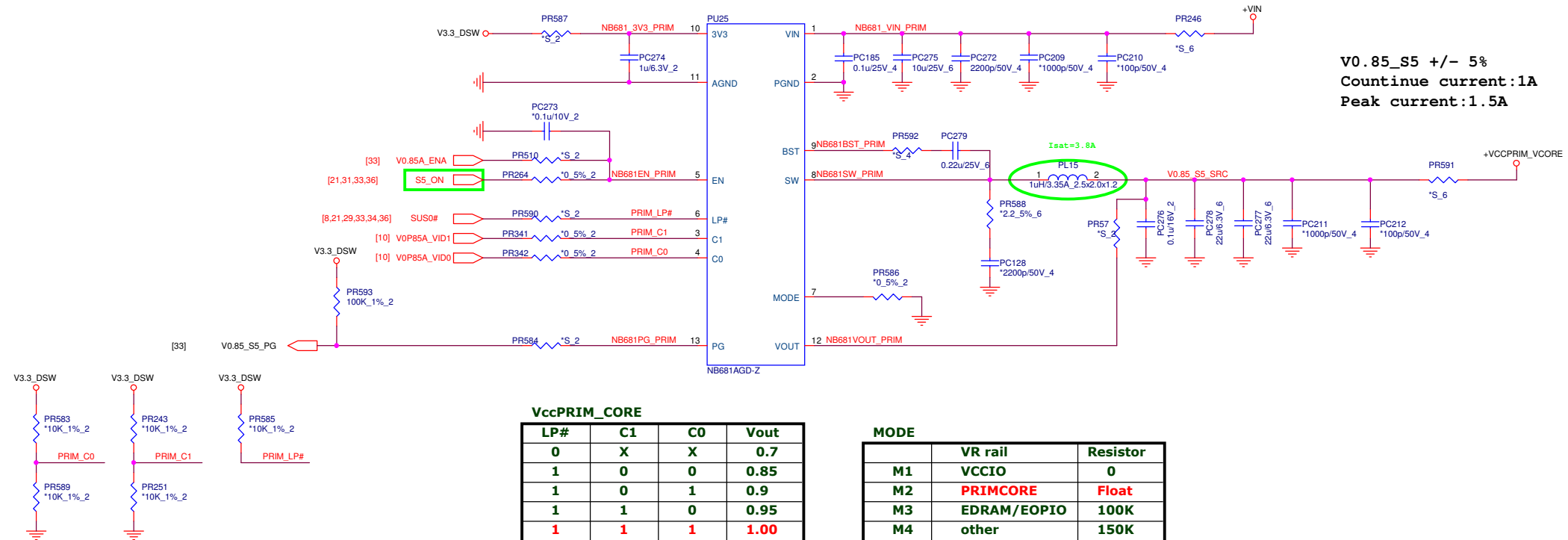


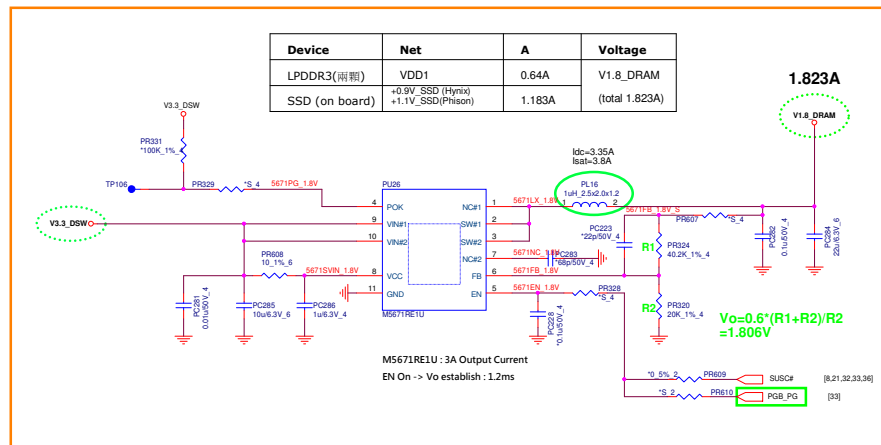


[15,28,29,30,31,32,33,34] +VIN

[10] +VCCPRIM_VCORE

[7,10,15,17,18,20,22,23,26,28,31,32,33,34,36] V3.3_DSW





17.11.8
Modify V1.8_DRAM from AOZ1331 to M5671